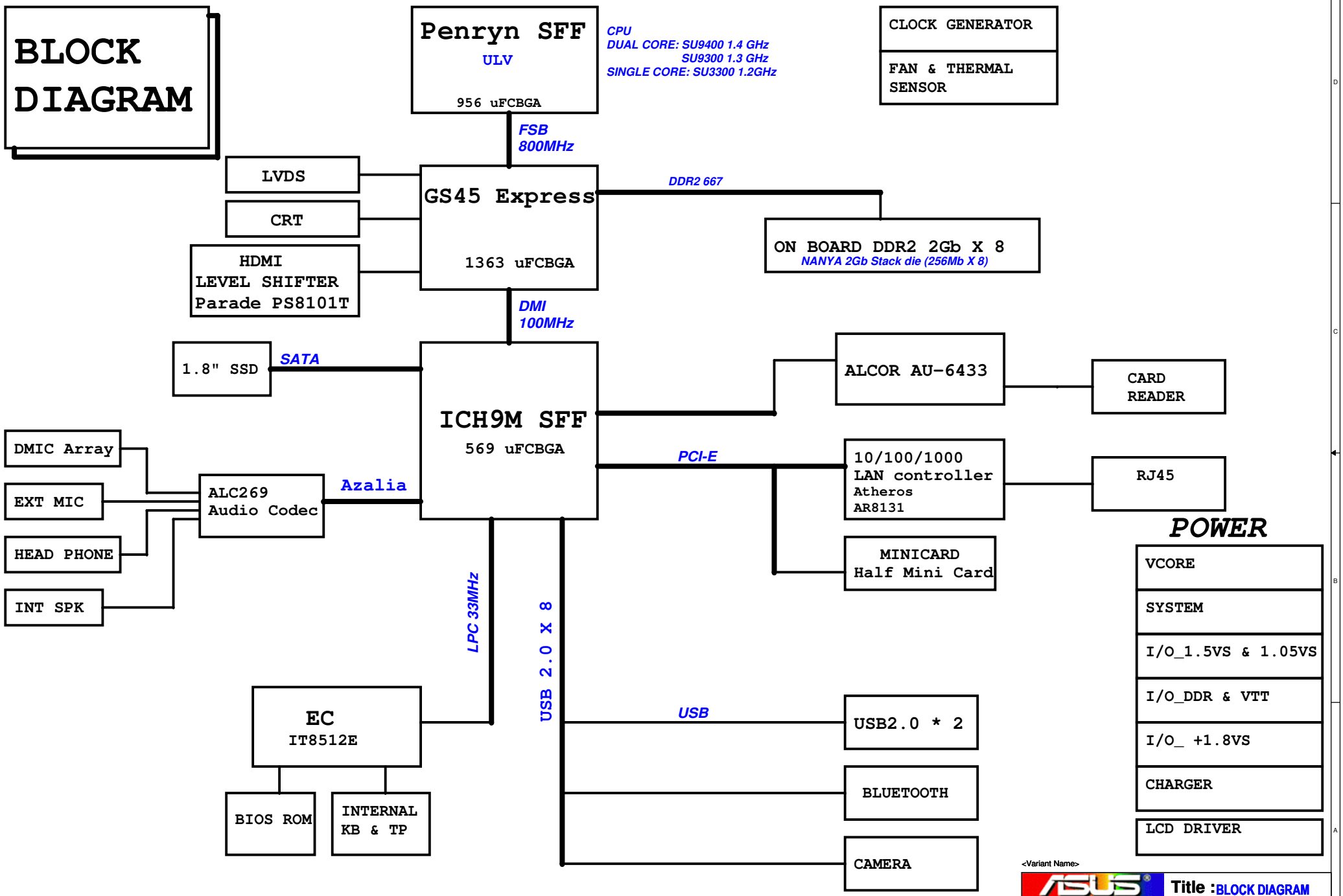


<Variant Name>

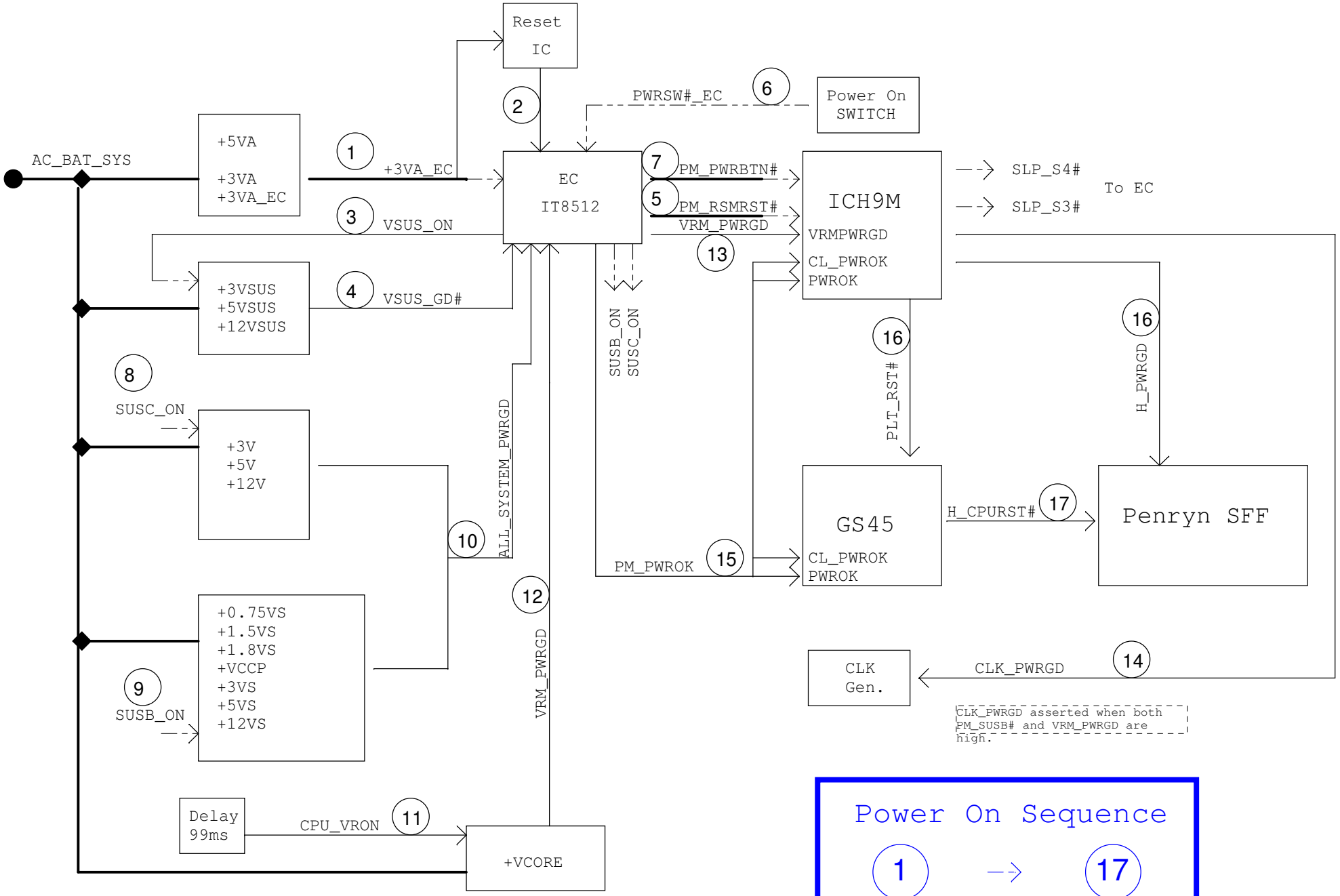
ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

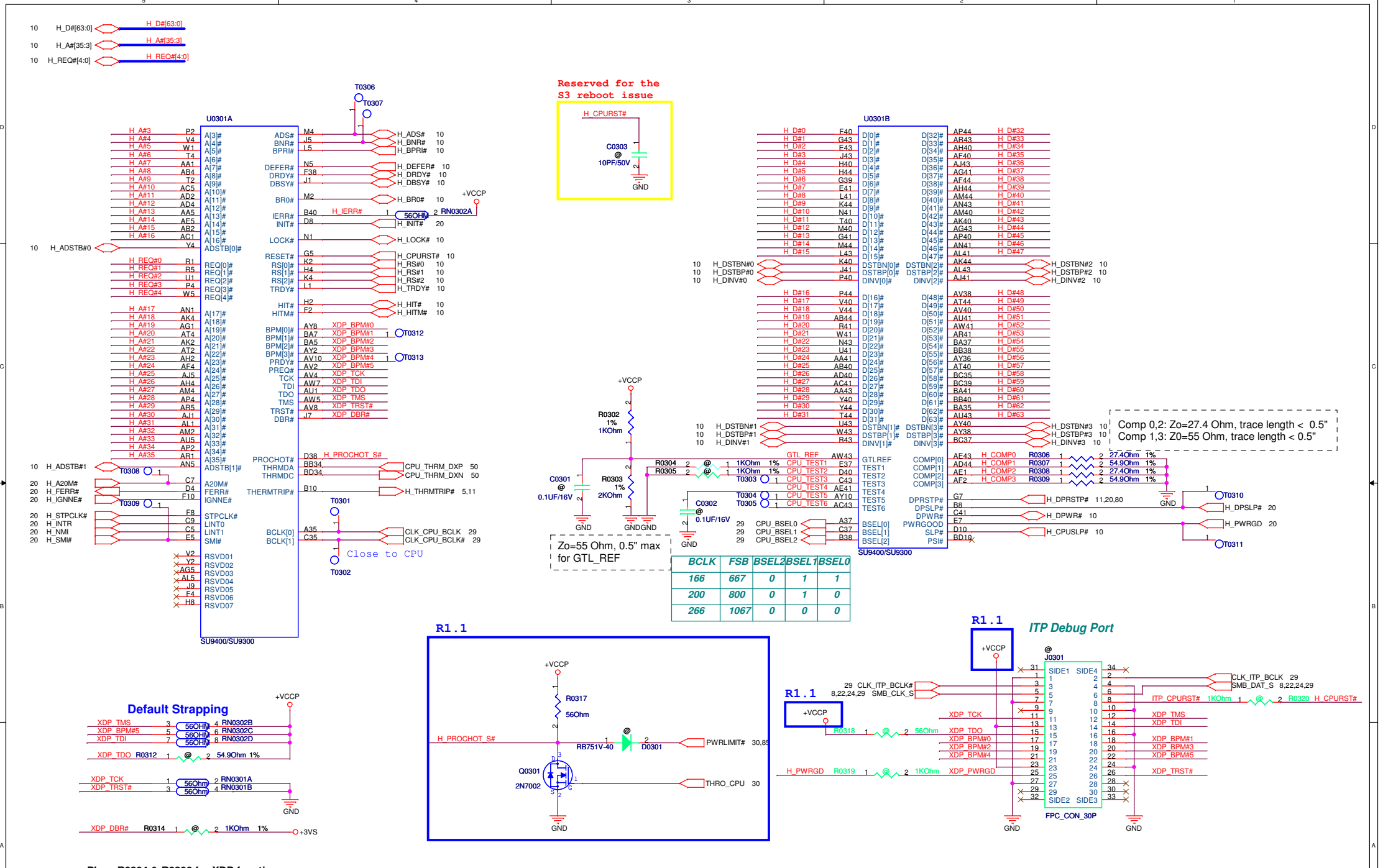
Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	1.4

Date: Monday, April 27, 2009 Sheet 1 of 93



ASUS	Title : POWER SEQUENCE		
<OrgName>	Engineer: Uei Lee & Hacken		
Size: Custom	Project Name: UX30 MB		Rev: 1.4
Date: Monday, April 27, 2009	Sheet 2 of 93		



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

<Variant Name>

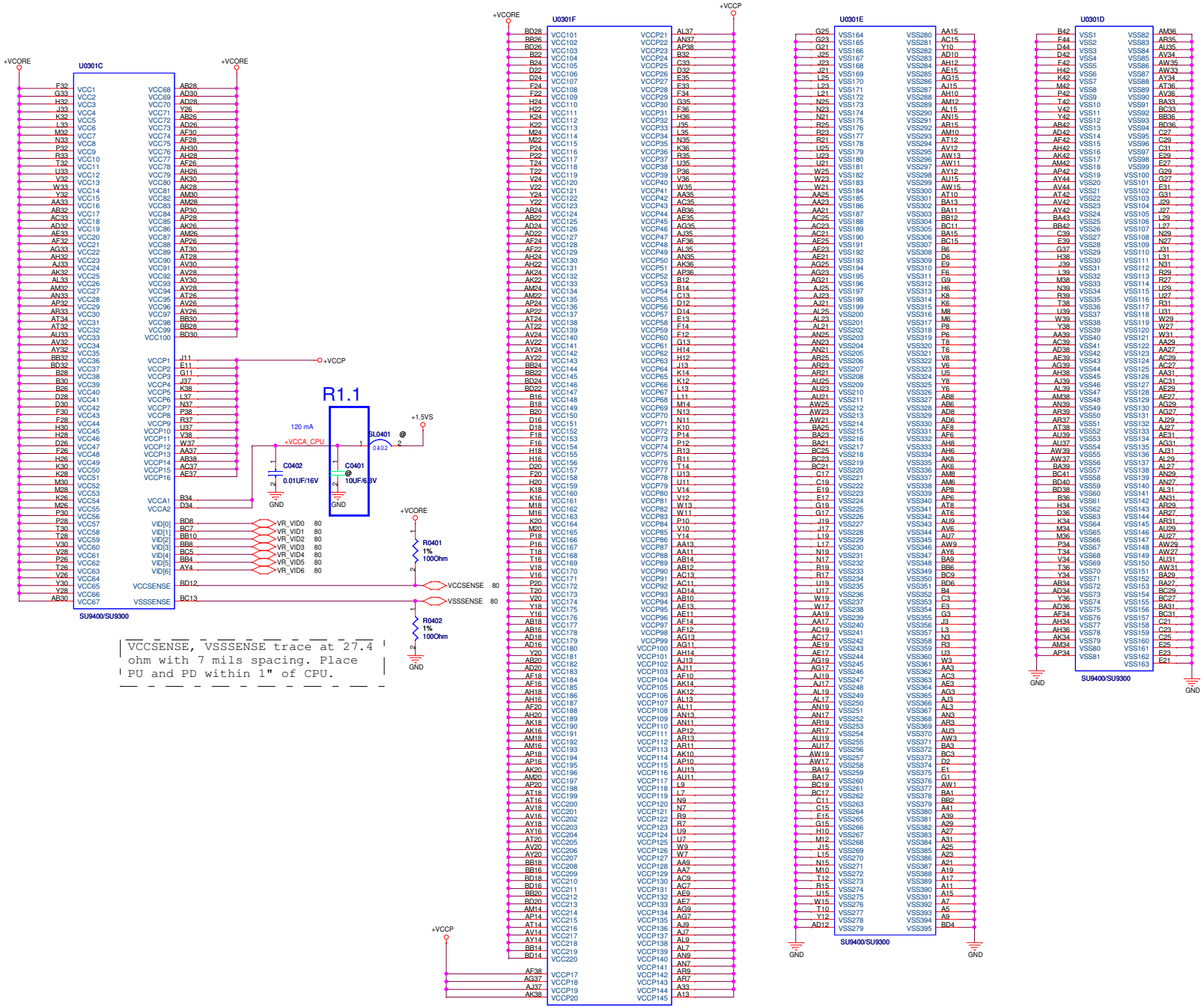
Title : CPU PENRYN ULV FSB

ASUSTeK COMPUTER INC

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	1.4

Date: Friday, May 08, 2009 Sheet 3 of 93



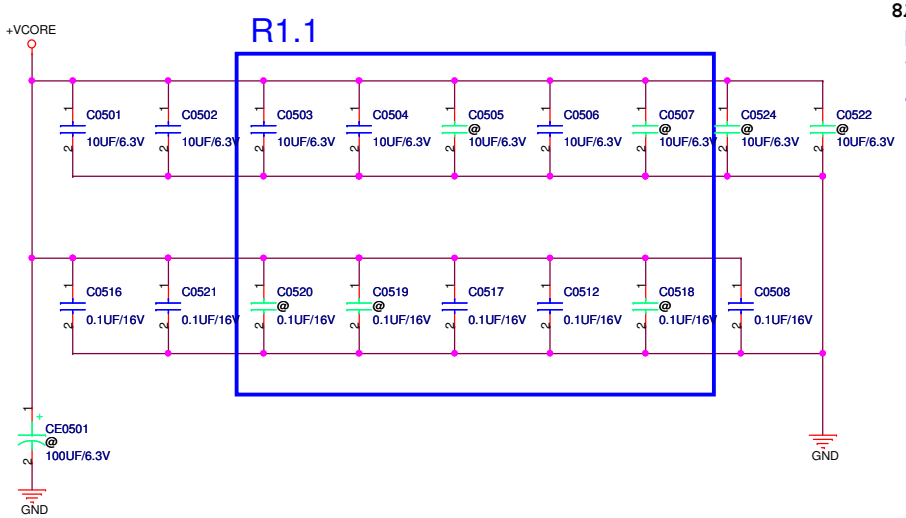
VCCSENSE, VSSSENSE trace at 27.4 ohm with 7 mils spacing. Place PU and PD within 1" of CPU.

8A for Ultra Low Voltage CPU TDP 10W

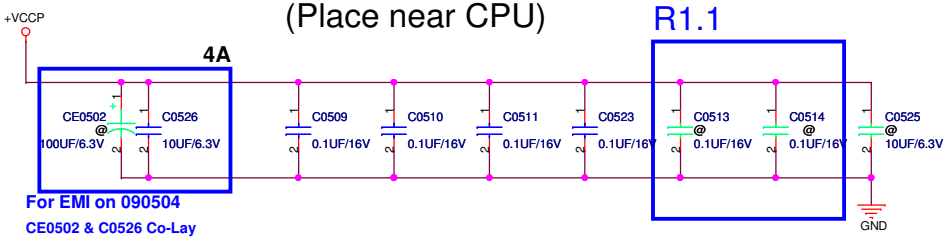
DESIGN IP VCORE

10UF X10

.1UF X 0



+VCCP Decoupling Capacitor (Place near CPU)



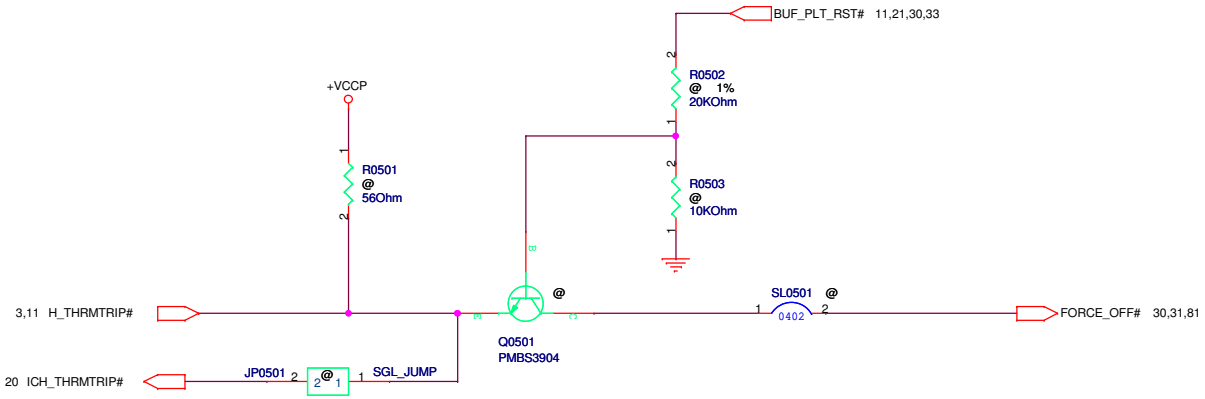
DESIGN IP VCCP

100UF X 1

10UF X 1

.1UF X 3

R1.1 FOLLOW DESIGN IP



Thermal Trip signal (From CPU to ICH-9M and sequence)

Decoupling guide from Intel

VCORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
VCCP	1uF	* 12pcs
	270uF	* 1pcs
VCCA	0.01uF	* 1 pcs
	10uF	* 1 pcs

<Variant Name>

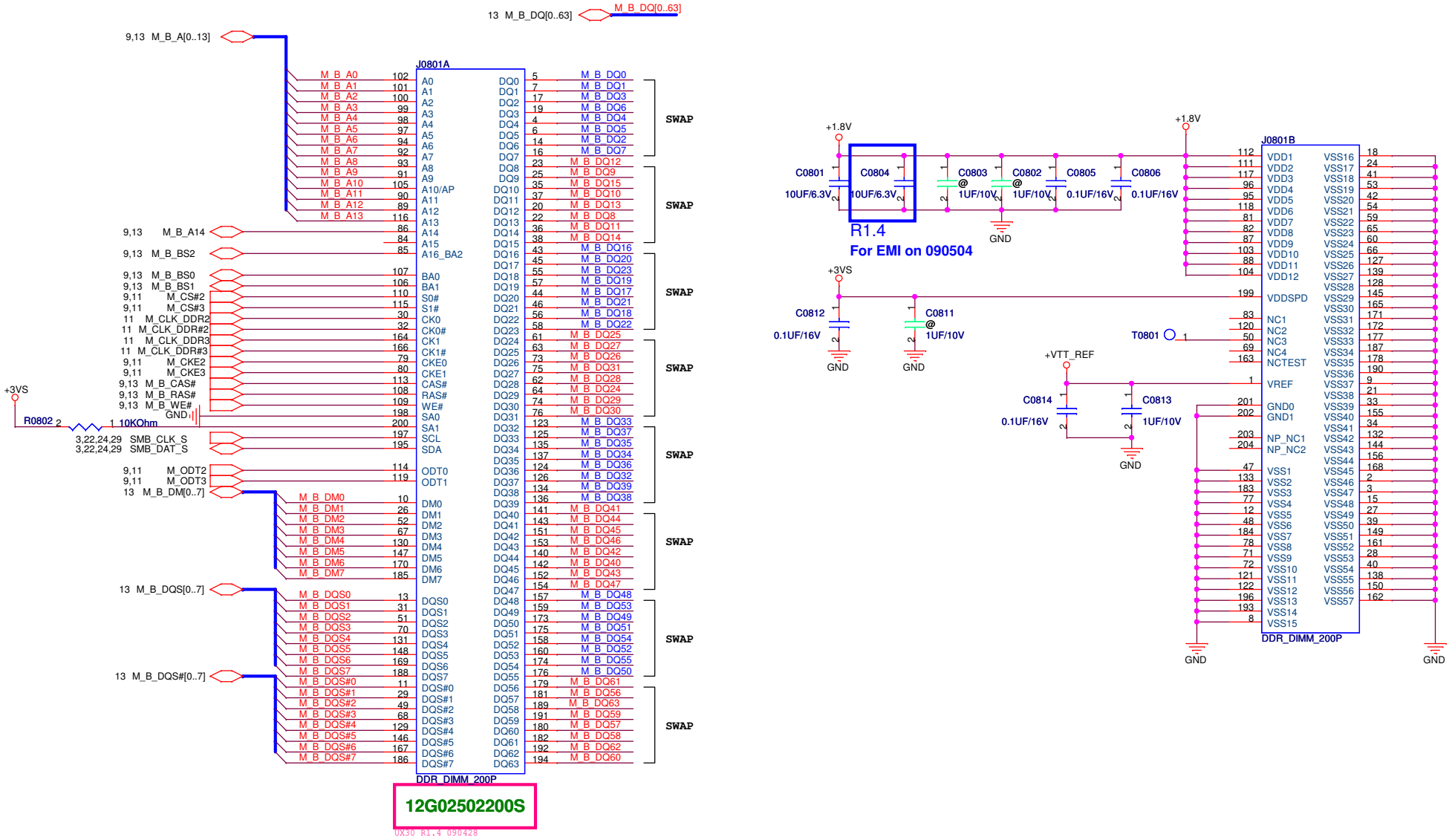
ASUSTeK COMPUTER INC	Title : CPU CAPACITORS	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 5 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 6 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title : SODIMM	
	Engineer: Uei Lee & Hacken	
Size: C	Project Name: UX30 MB	Rev: 1.4
Date: Tuesday, April 28, 2009	Sheet 7 of 93	



<Variant Name>

ASUSTeK COMPUTER INC

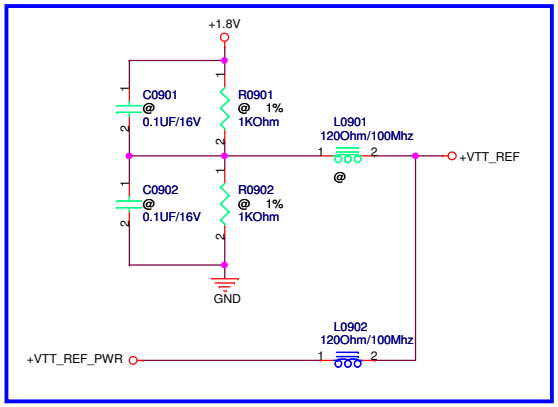
Title : M DDR3 SP-DIMM CHANNEL B

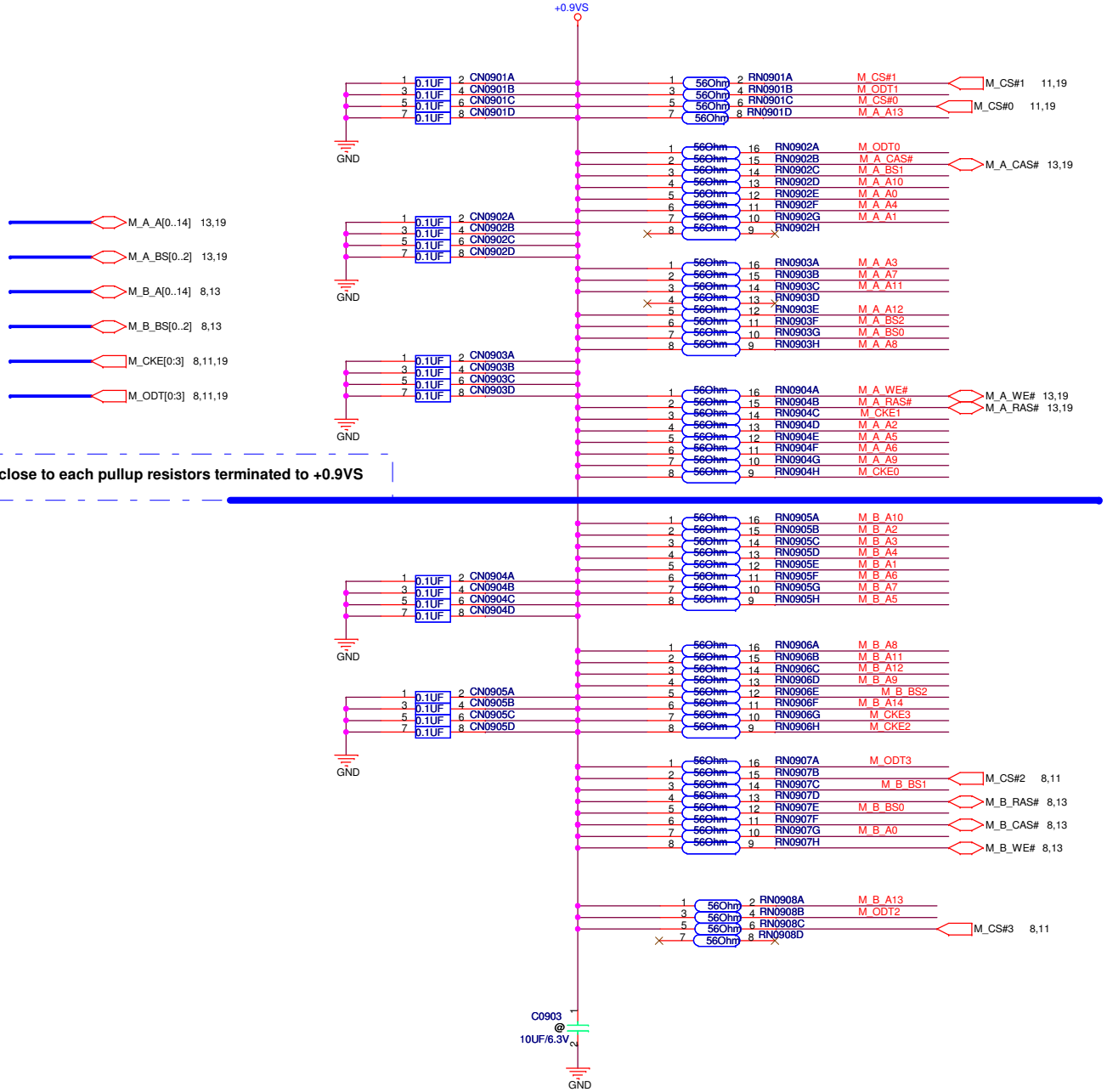
Engineer: UEI

Size	Project Name	Rev
B	UX30 MB	1.4

Date: Friday, May 08, 2009 Sheet 8 of 93

R1.1

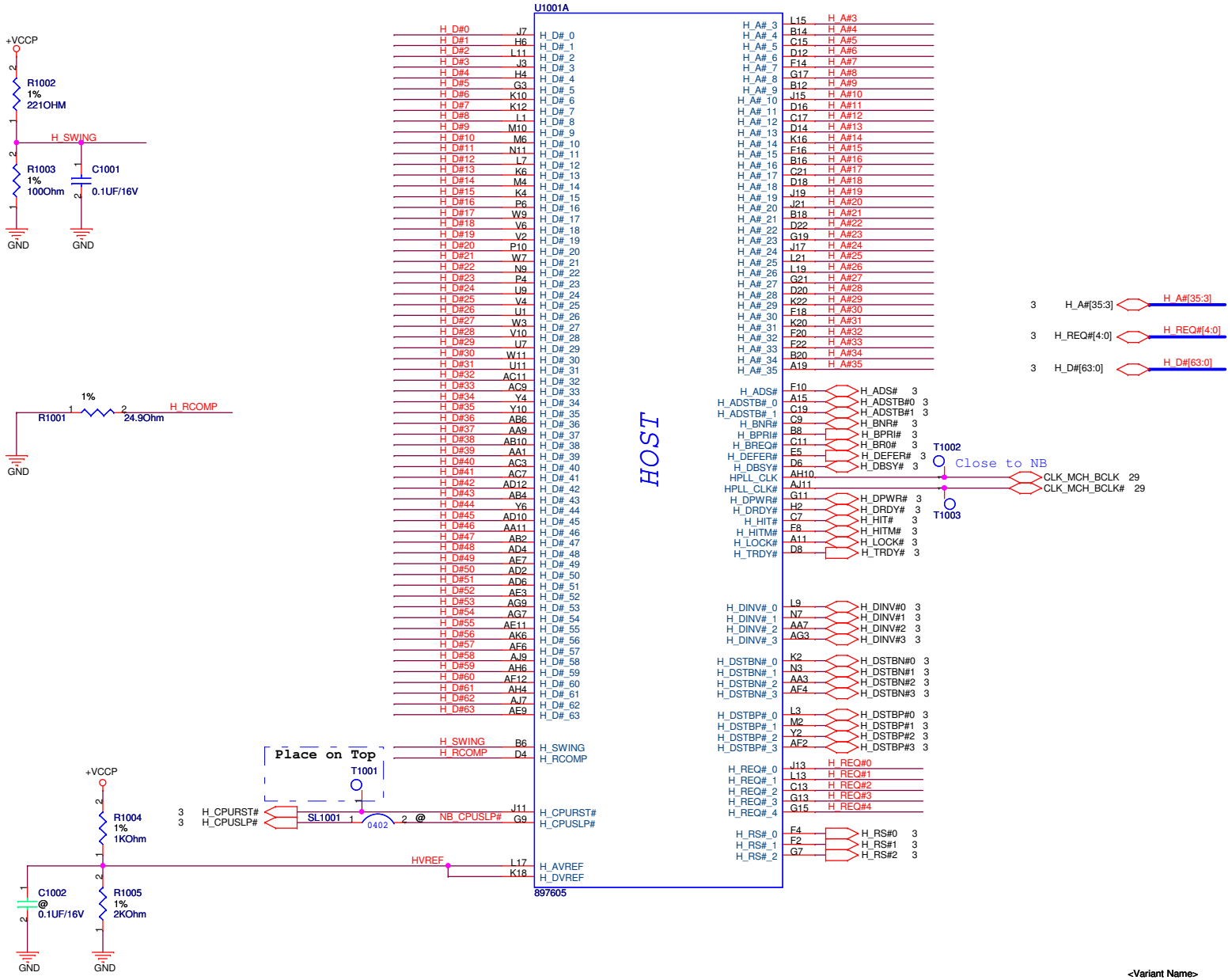




Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

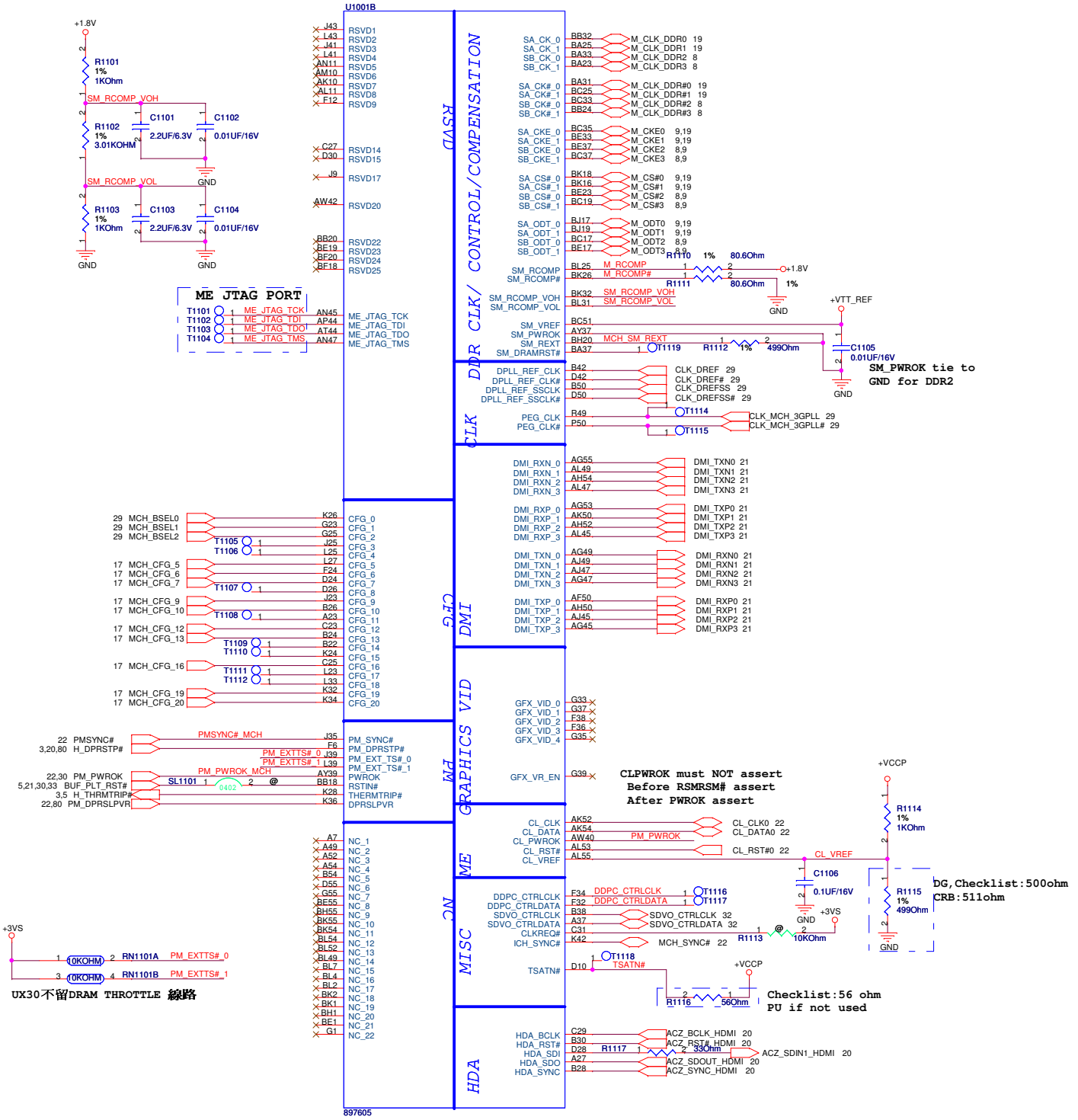
<Variant Name>

ASUSTeK COMPUTER INC	Title : DIM DDR2 VREF	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 9 of 93	



<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 HOST	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 10 of 93	



<Variant Name>

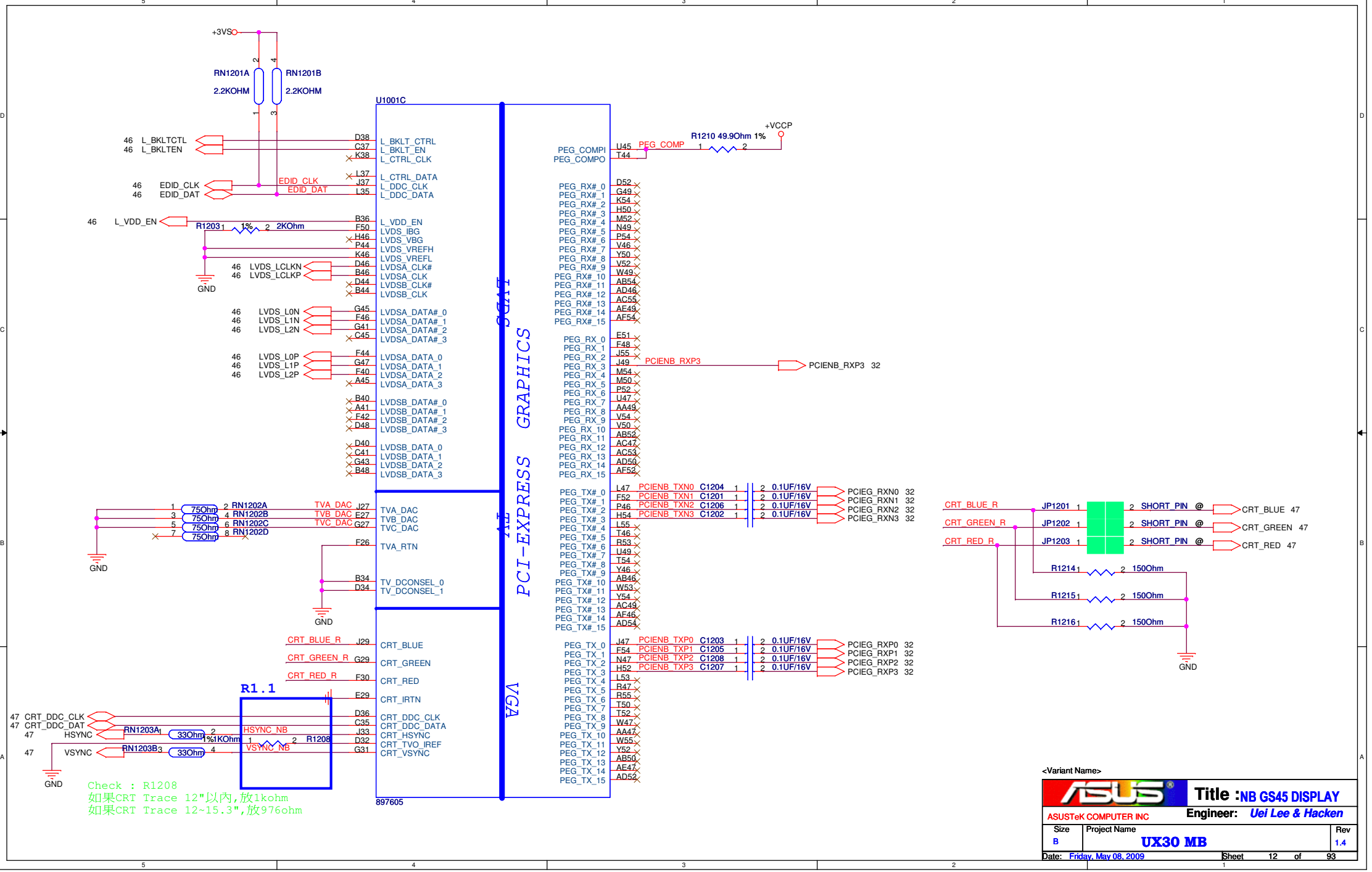
ASUSTeK COMPUTER INC

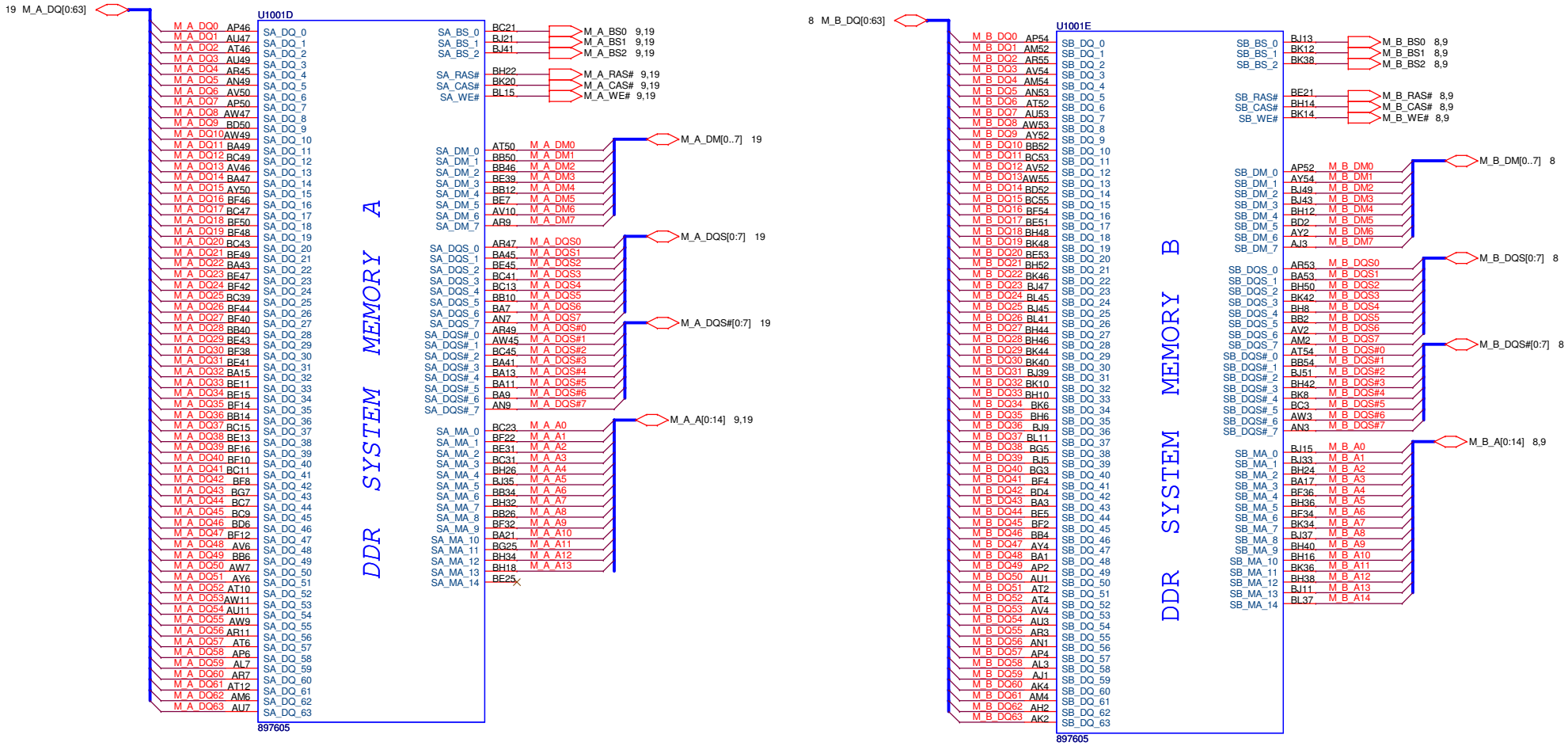
Title : NB GS45 DMI

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	1.4

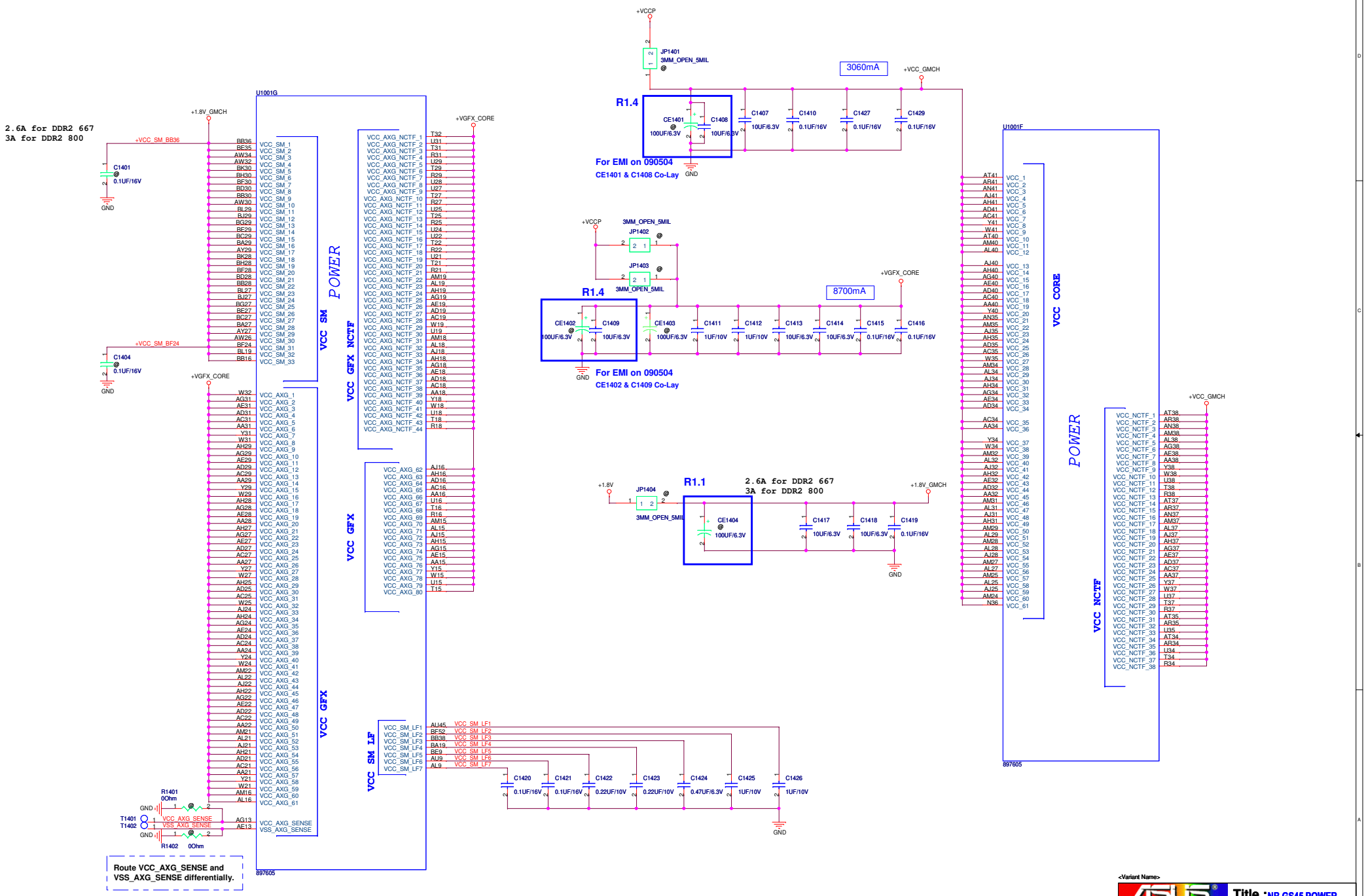
Date: Friday, May 08, 2009 Sheet 11 of 93

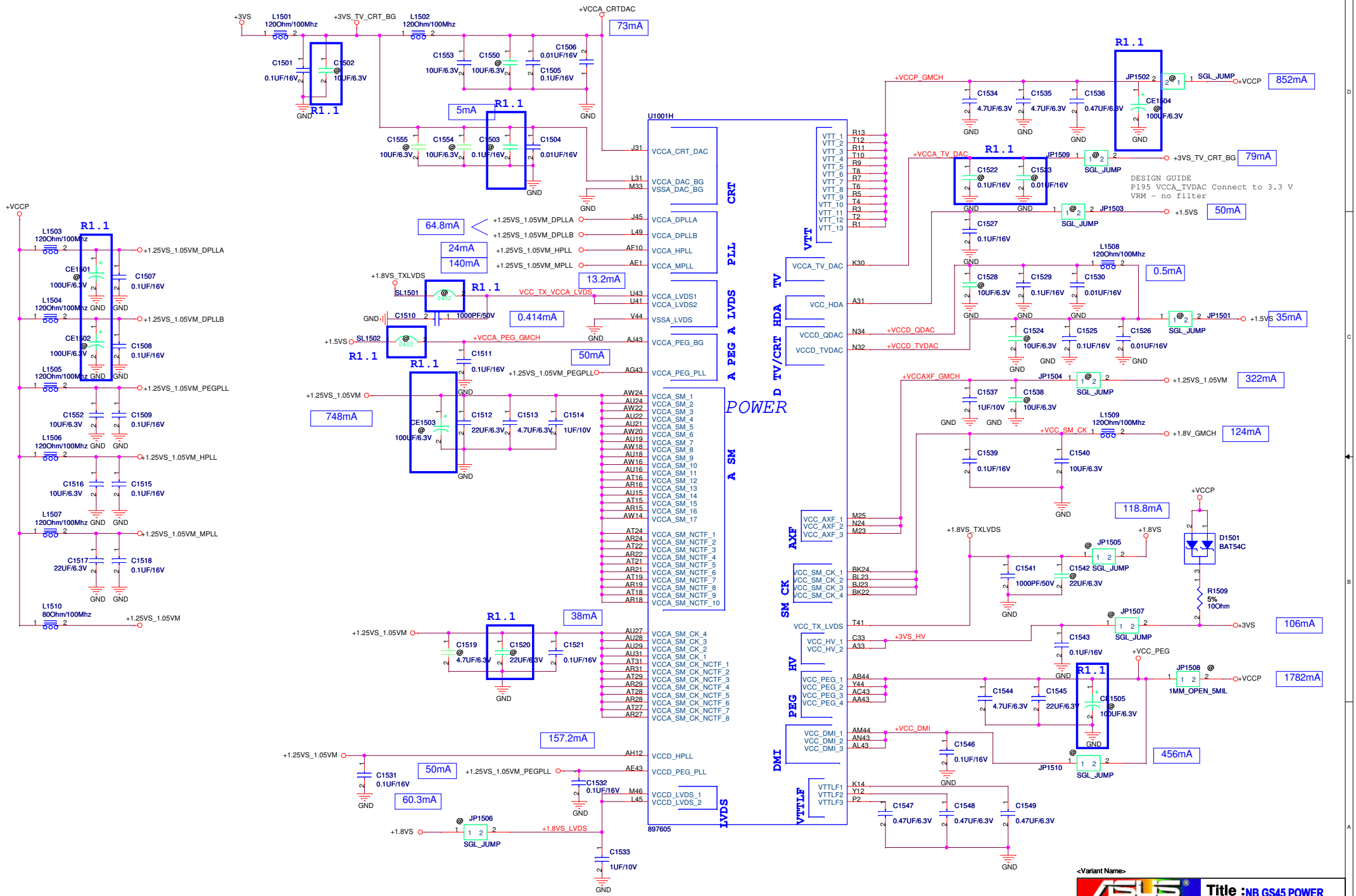

U1001C
PCI-EXPRESS GRAPHICS
LVDS
TV
VGA
+3VS
RN1201A 2.2KOHM
RN1201B 2.2KOHM
46 L_BKLTCTL
46 L_BKLTEN
46 EDID_CLK
46 EDID_DAT
46 L_VDD_EN
R1203 1% 2KOhm
GND
46 LVDS_LCLKN
46 LVDS_LCLKP
46 LVDS_L0N
46 LVDS_L1N
46 LVDS_L2N
46 LVDS_L0P
46 LVDS_L1P
46 LVDS_L2P
RN1202A 75Ohm
RN1202B 75Ohm
RN1202C 75Ohm
RN1202D 75Ohm
TVA_DAC
TVB_DAC
TVC_DAC
TVA_RTN
TV_DCONSEL_0
TV_DCONSEL_1
CRT_BLUE_R
CRT_GREEN_R
CRT_RED_R
R1.1
47 CRT_DDC_CLK
47 CRT_DDC_DAT
47 HSYNC
47 VSYNC
RN1203A 33Ohm
RN1203B 33Ohm
HSYNC_NB
VSYNC_NB
R1208 1%1KOhm
CRT_IRTN
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC
897605
L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA
L_VDD_EN
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
LVDSA_DATA#_3
LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
LVDSA_DATA_3
LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
LVDSB_DATA#_3
LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
LVDSB_DATA_3
PEG_COMPI
PEG_COMPO
PEG_COMP
R1210 49.9Ohm 1%
+VCCP
PEG_RX#_0
PEG_RX#_1
PEG_RX#_2
PEG_RX#_3
PEG_RX#_4
PEG_RX#_5
PEG_RX#_6
PEG_RX#_7
PEG_RX#_8
PEG_RX#_9
PEG_RX#_10
PEG_RX#_11
PEG_RX#_12
PEG_RX#_13
PEG_RX#_14
PEG_RX#_15
PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15
PCIENB_RXP3
PCIENB_RXP3 32
PEG_TX#_0
PEG_TX#_1
PEG_TX#_2
PEG_TX#_3
PEG_TX#_4
PEG_TX#_5
PEG_TX#_6
PEG_TX#_7
PEG_TX#_8
PEG_TX#_9
PEG_TX#_10
PEG_TX#_11
PEG_TX#_12
PEG_TX#_13
PEG_TX#_14
PEG_TX#_15
PCIENB_TXN0 C1204 0.1UF/16V
PCIENB_TXN1 C1201 0.1UF/16V
PCIENB_TXN2 C1206 0.1UF/16V
PCIENB_TXN3 C1202 0.1UF/16V
PCIEG_RXN0 32
PCIEG_RXN1 32
PCIEG_RXN2 32
PCIEG_RXN3 32
PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15
PCIENB_TXP0 C1203 0.1UF/16V
PCIENB_TXP1 C1205 0.1UF/16V
PCIENB_TXP2 C1208 0.1UF/16V
PCIENB_TXP3 C1207 0.1UF/16V
PCIEG_RXP0 32
PCIEG_RXP1 32
PCIEG_RXP2 32
PCIEG_RXP3 32
CRT_BLUE_R
CRT_GREEN_R
CRT_RED_R
JP1201 SHORT_PIN @
JP1202 SHORT_PIN @
JP1203 SHORT_PIN @
CRT_BLUE 47
CRT_GREEN 47
CRT_RED 47
R1214 150Ohm
R1215 150Ohm
R1216 150Ohm
GND
Check : R1208
如果CRT Trace 12"以內,放1kohm
如果CRT Trace 12~15.3",放976ohm
<Variant Name>
Title :NB GS45 DISPLAY
ASUSTeK COMPUTER INC
Engineer: Uei Lee & Hacken
Size B
Project Name UX30 MB
Rev 1.4
Date: Friday, May 08, 2009
Sheet 12 of 93



<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 DDR3 BUS	Engineer: Uei Lee & Hacken
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 13 of 93	


2.6A for DDR2 667
3A for DDR2 800
U1001G
+1.8V_GMCH
+VCC_SM_BB36
+VCC_SM_BF24
C1401 @ 0.1UF/16V
C1404 @ 0.1UF/16V
GND
VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33
VCC SM POWER
+VGFX_CORE
VCC_AXG_1 VCC_AXG_2 VCC_AXG_3 VCC_AXG_4 VCC_AXG_5 VCC_AXG_6 VCC_AXG_7 VCC_AXG_8 VCC_AXG_9 VCC_AXG_10 VCC_AXG_11 VCC_AXG_12 VCC_AXG_13 VCC_AXG_14 VCC_AXG_15 VCC_AXG_16 VCC_AXG_17 VCC_AXG_18 VCC_AXG_19 VCC_AXG_20 VCC_AXG_21 VCC_AXG_22 VCC_AXG_23 VCC_AXG_24 VCC_AXG_25 VCC_AXG_26 VCC_AXG_27 VCC_AXG_28 VCC_AXG_29 VCC_AXG_30 VCC_AXG_31 VCC_AXG_32 VCC_AXG_33 VCC_AXG_34 VCC_AXG_35 VCC_AXG_36 VCC_AXG_37 VCC_AXG_38 VCC_AXG_39 VCC_AXG_40 VCC_AXG_41 VCC_AXG_42 VCC_AXG_43 VCC_AXG_44 VCC_AXG_45 VCC_AXG_46 VCC_AXG_47 VCC_AXG_48 VCC_AXG_49 VCC_AXG_50 VCC_AXG_51 VCC_AXG_52 VCC_AXG_53 VCC_AXG_54 VCC_AXG_55 VCC_AXG_56 VCC_AXG_57 VCC_AXG_58 VCC_AXG_59 VCC_AXG_60 VCC_AXG_61
VCC GFX
VCC_AXG_NCTF_1 VCC_AXG_NCTF_2 VCC_AXG_NCTF_3 VCC_AXG_NCTF_4 VCC_AXG_NCTF_5 VCC_AXG_NCTF_6 VCC_AXG_NCTF_7 VCC_AXG_NCTF_8 VCC_AXG_NCTF_9 VCC_AXG_NCTF_10 VCC_AXG_NCTF_11 VCC_AXG_NCTF_12 VCC_AXG_NCTF_13 VCC_AXG_NCTF_14 VCC_AXG_NCTF_15 VCC_AXG_NCTF_16 VCC_AXG_NCTF_17 VCC_AXG_NCTF_18 VCC_AXG_NCTF_19 VCC_AXG_NCTF_20 VCC_AXG_NCTF_21 VCC_AXG_NCTF_22 VCC_AXG_NCTF_23 VCC_AXG_NCTF_24 VCC_AXG_NCTF_25 VCC_AXG_NCTF_26 VCC_AXG_NCTF_27 VCC_AXG_NCTF_28 VCC_AXG_NCTF_29 VCC_AXG_NCTF_30 VCC_AXG_NCTF_31 VCC_AXG_NCTF_32 VCC_AXG_NCTF_33 VCC_AXG_NCTF_34 VCC_AXG_NCTF_35 VCC_AXG_NCTF_36 VCC_AXG_NCTF_37 VCC_AXG_NCTF_38 VCC_AXG_NCTF_39 VCC_AXG_NCTF_40 VCC_AXG_NCTF_41 VCC_AXG_NCTF_42 VCC_AXG_NCTF_43 VCC_AXG_NCTF_44
VCC GFX NCTF
VCC_AXG_62 VCC_AXG_63 VCC_AXG_64 VCC_AXG_65 VCC_AXG_66 VCC_AXG_67 VCC_AXG_68 VCC_AXG_69 VCC_AXG_70 VCC_AXG_71 VCC_AXG_72 VCC_AXG_73 VCC_AXG_74 VCC_AXG_75 VCC_AXG_76 VCC_AXG_77 VCC_AXG_78 VCC_AXG_79 VCC_AXG_80
VCC_SM_LF1 VCC_SM_LF2 VCC_SM_LF3 VCC_SM_LF4 VCC_SM_LF5 VCC_SM_LF6 VCC_SM_LF7
VCC SM LF
C1420 0.1UF/16V
C1421 0.1UF/16V
C1422 0.22UF/10V
C1423 0.22UF/10V
C1424 0.47UF/6.3V
C1425 1UF/10V
C1426 1UF/10V
R1401 0Ohm
R1402 0Ohm
T1401 VCC_AXG_SENSE
T1402 VSS_AXG_SENSE
Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.
897605
+VCCP
JP1401 3MM_OPEN_5MIL
3060mA
+VCC_GMCH
R1.4
CE1401 @ 100UF/6.3V
C1408 10UF/6.3V
C1407 10UF/6.3V
C1410 0.1UF/16V
C1427 0.1UF/16V
C1429 0.1UF/16V
For EMI on 090504
CE1401 & C1408 Co-Lay
JP1402 @
JP1403 @
3MM_OPEN_5MIL
8700mA
CE1402 @ 100UF/6.3V
C1409 10UF/6.3V
CE1403 @ 100UF/6.3V
C1411 1UF/10V
C1412 1UF/10V
C1413 10UF/6.3V
C1414 10UF/6.3V
C1415 0.1UF/16V
C1416 0.1UF/16V
For EMI on 090504
CE1402 & C1409 Co-Lay
+1.8V
JP1404 @
3MM_OPEN_5MIL
R1.1
2.6A for DDR2 667
3A for DDR2 800
+1.8V_GMCH
CE1404 @ 100UF/6.3V
C1417 10UF/6.3V
C1418 10UF/6.3V
C1419 0.1UF/16V
U1001F
VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35 VCC_36 VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61
VCC CORE POWER
VCC_NCTF_1 VCC_NCTF_2 VCC_NCTF_3 VCC_NCTF_4 VCC_NCTF_5 VCC_NCTF_6 VCC_NCTF_7 VCC_NCTF_8 VCC_NCTF_9 VCC_NCTF_10 VCC_NCTF_11 VCC_NCTF_12 VCC_NCTF_13 VCC_NCTF_14 VCC_NCTF_15 VCC_NCTF_16 VCC_NCTF_17 VCC_NCTF_18 VCC_NCTF_19 VCC_NCTF_20 VCC_NCTF_21 VCC_NCTF_22 VCC_NCTF_23 VCC_NCTF_24 VCC_NCTF_25 VCC_NCTF_26 VCC_NCTF_27 VCC_NCTF_28 VCC_NCTF_29 VCC_NCTF_30 VCC_NCTF_31 VCC_NCTF_32 VCC_NCTF_33 VCC_NCTF_34 VCC_NCTF_35 VCC_NCTF_36 VCC_NCTF_37 VCC_NCTF_38
VCC NCTF
897605



<Variant Name>

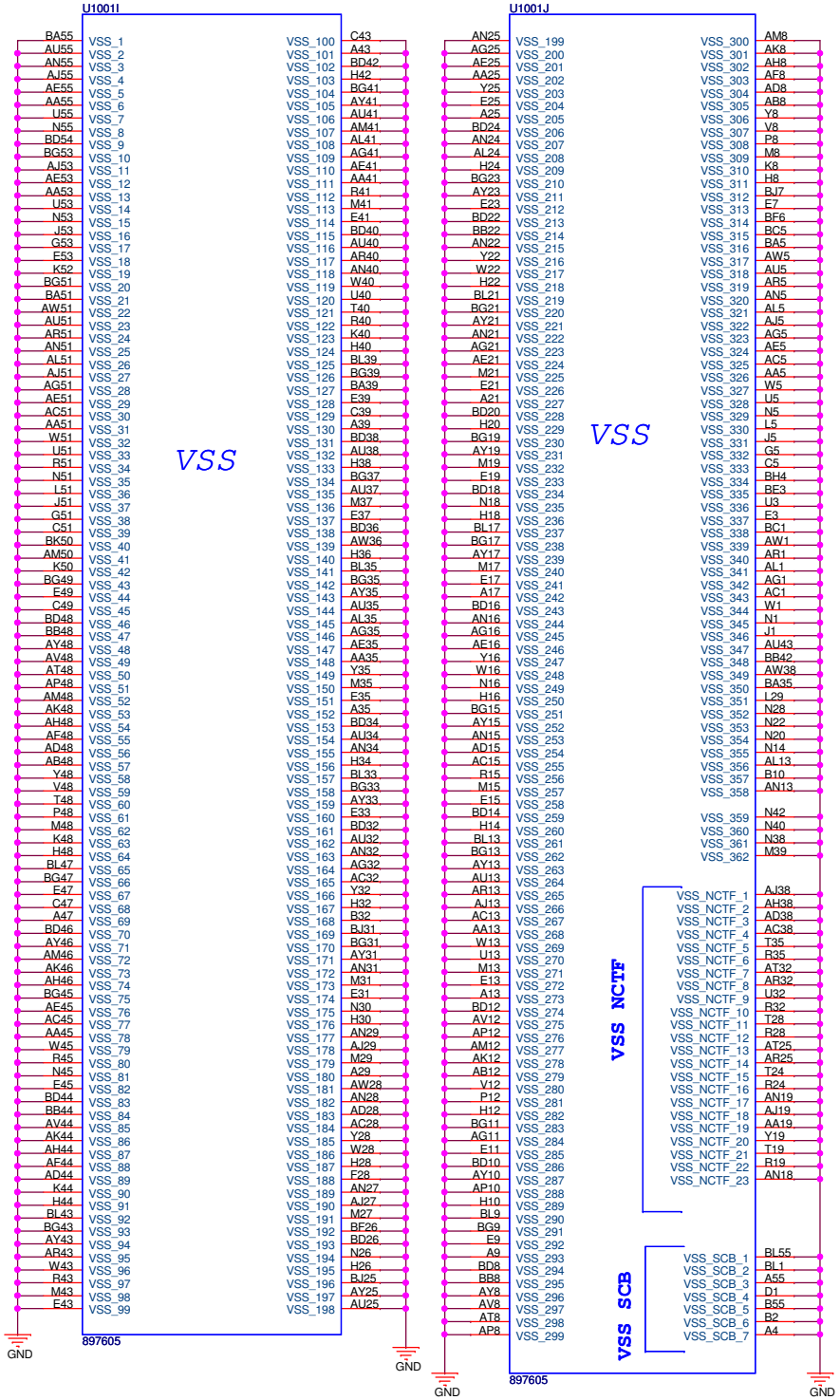
ASUSTeK COMPUTER INC

Title : NB GS45 POWER

Engineer: Uei Lee & Hacken

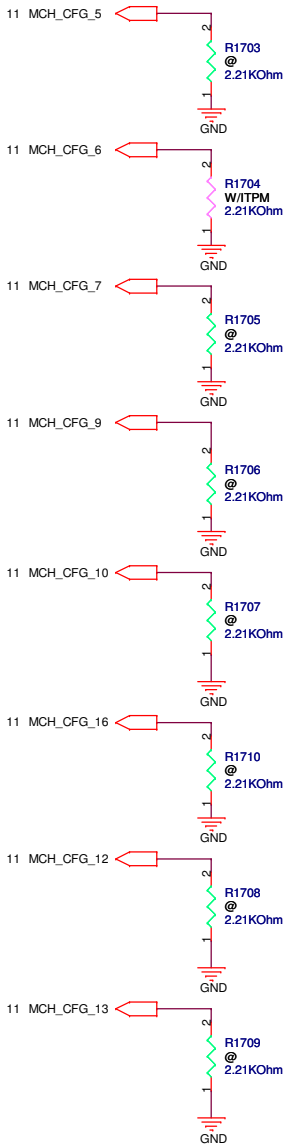
Size	Project Name	Rev
Custom	UX30 MB	1.4

Date: Wednesday, May 06, 2009 Sheet 15 of 93



<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 GND	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 16 of 93	



CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface (Relate to SPI_MOSI)
H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)

CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse

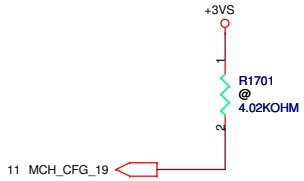
CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable

CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

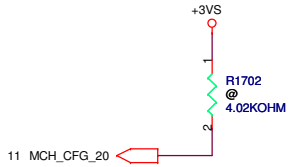
CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)



CFG19 : DMI Lane Reversal

H =DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE

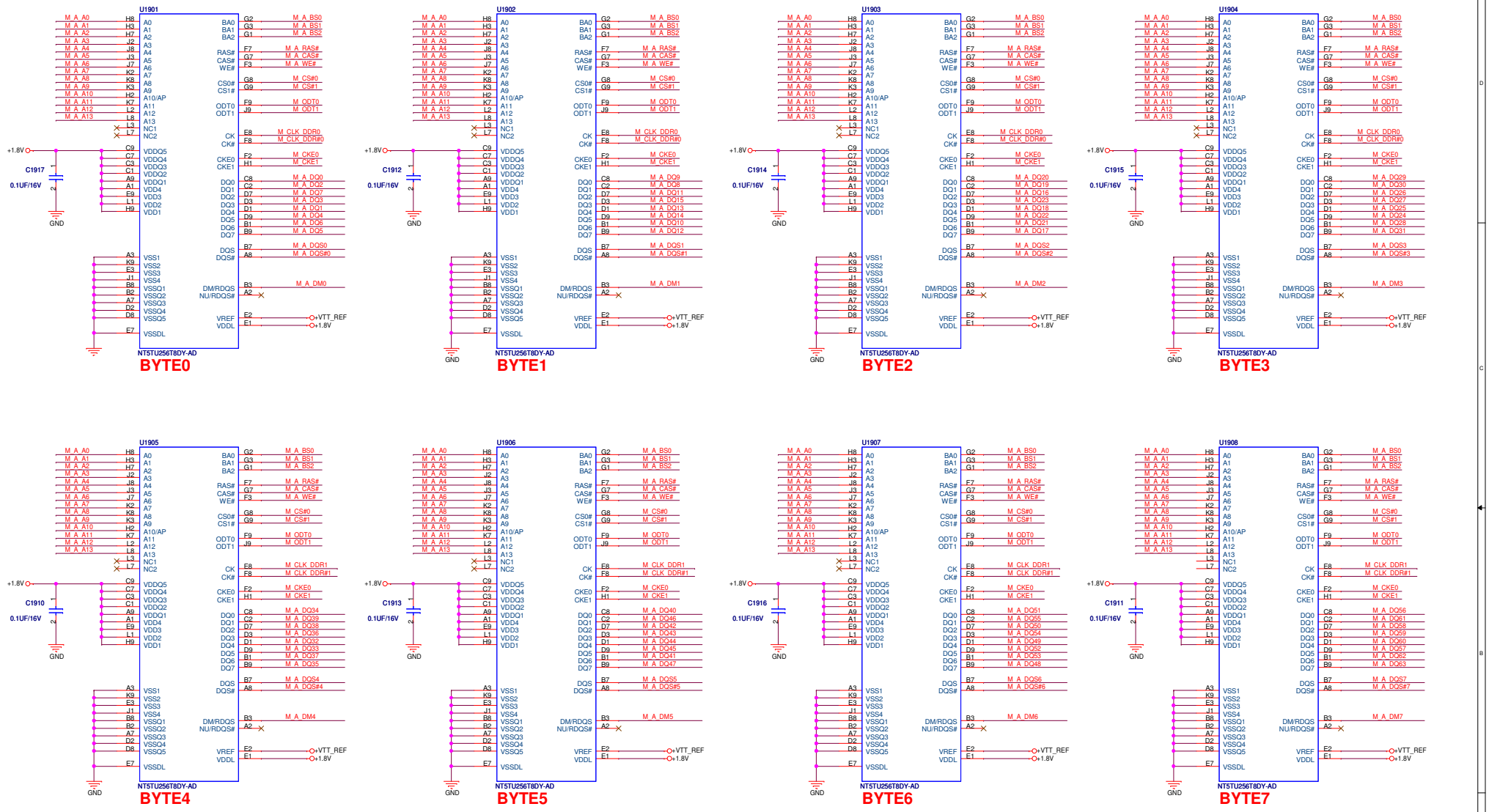
L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>

ASUSTeK COMPUTER INC	Title : NB GS45 STRAPPING	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 17 of 93	

<Variant Name>

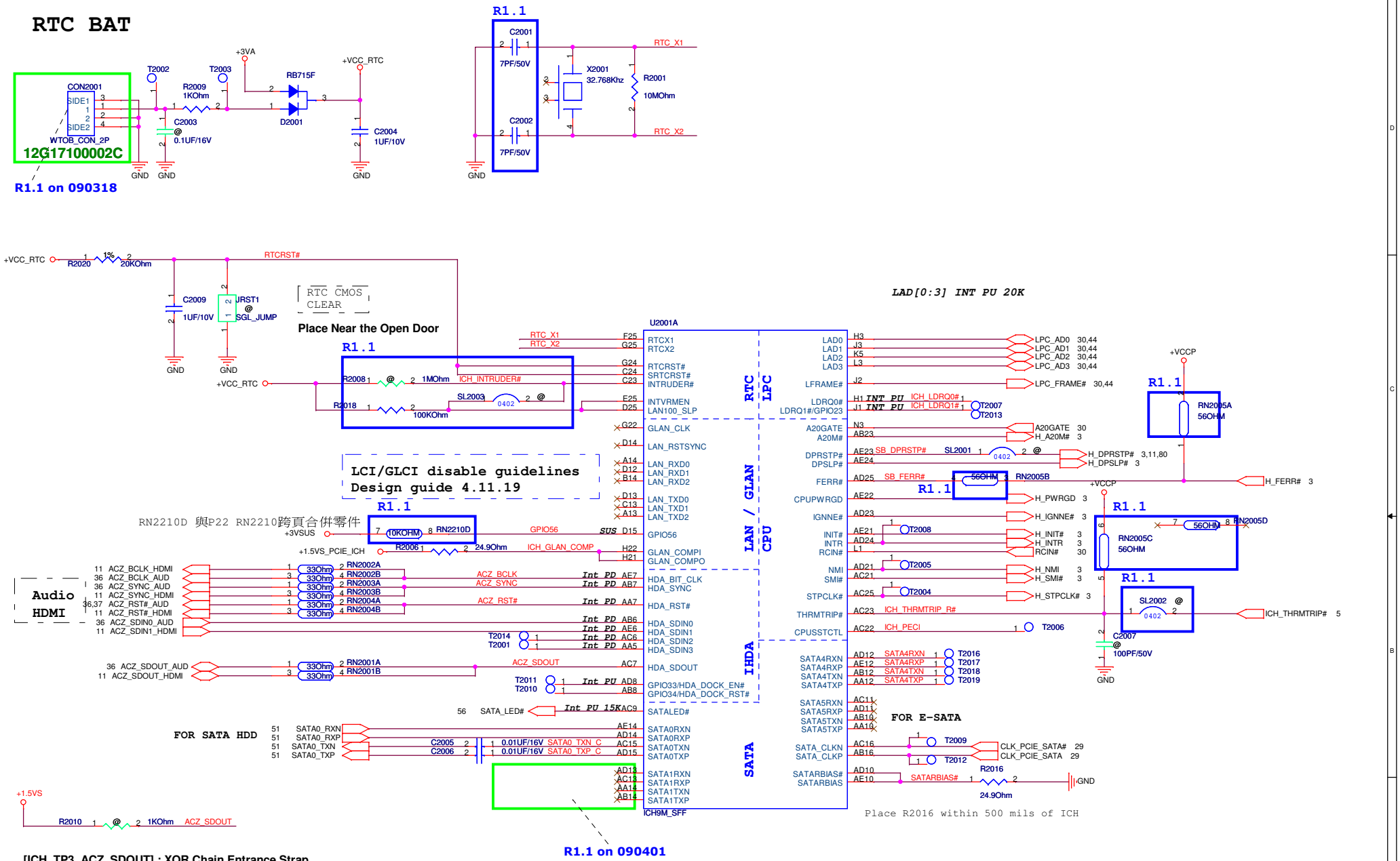
ASUS	Title :*	
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 1.4
Date: Monday, April 27, 2009	Sheet 18 of 93	



<Variant Name>

ASUSTeK COMPUTER INC	Title : On Board RAM	
	Engineer: Uei Lee & Hacken	
Size: C	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 19 of 93	

RTC BAT



[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

00 = Reserved

01= Enter XOR Chain

10= Normal Operation (Default)

11= Set PCIe Port Config Bit 1

GPIO33:Flash Descriptor Security Override

High = Enable (Default)
Low = Overridden

<Variant Name>

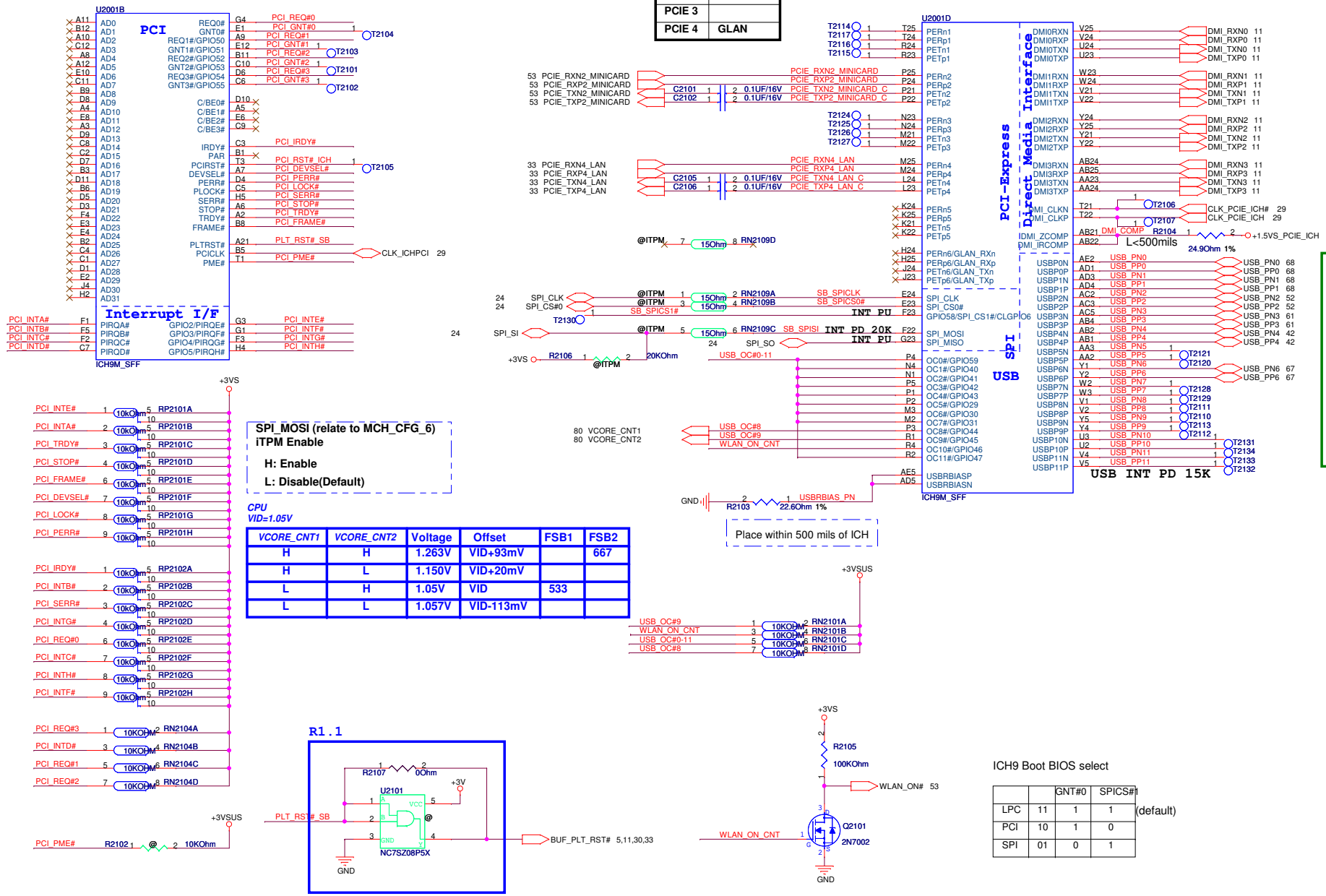
ASUSTeK COMPUTER INC

Title : SB ICH9M PCI PCIE DMI USB

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	1.4

Date: Friday, May 08, 2009 Sheet 20 of 93



PCIE 1	
PCIE 2	WLAN
PCIE 3	
PCIE 4	GLAN

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	Bluetooth
USB 4	Card Reader
USB 5	X
USB 6	CMOS Camera
USB 7	X
USB 8	X
USB 9	X
USB 10	3G CARD
USB 11	X

SPI_MOSI (relate to MCH_CFG_6)
iTPM Enable

H: Enable

L: Disable(Default)

CPU
VID=1.05V

VCORE_CNT1	VCORE_CNT2	Voltage	Offset	FSB1	FSB2
H	H	1.263V	VID+93mV		667
H	L	1.150V	VID+20mV		
L	H	1.05V	VID	533	
L	L	1.057V	VID-113mV		

ICH9 Boot BIOS select

		GNT#0	SPICS#1
LPC	11	1	1 (default)
PCI	10	1	0
SPI	01	0	1

<Variant Name>

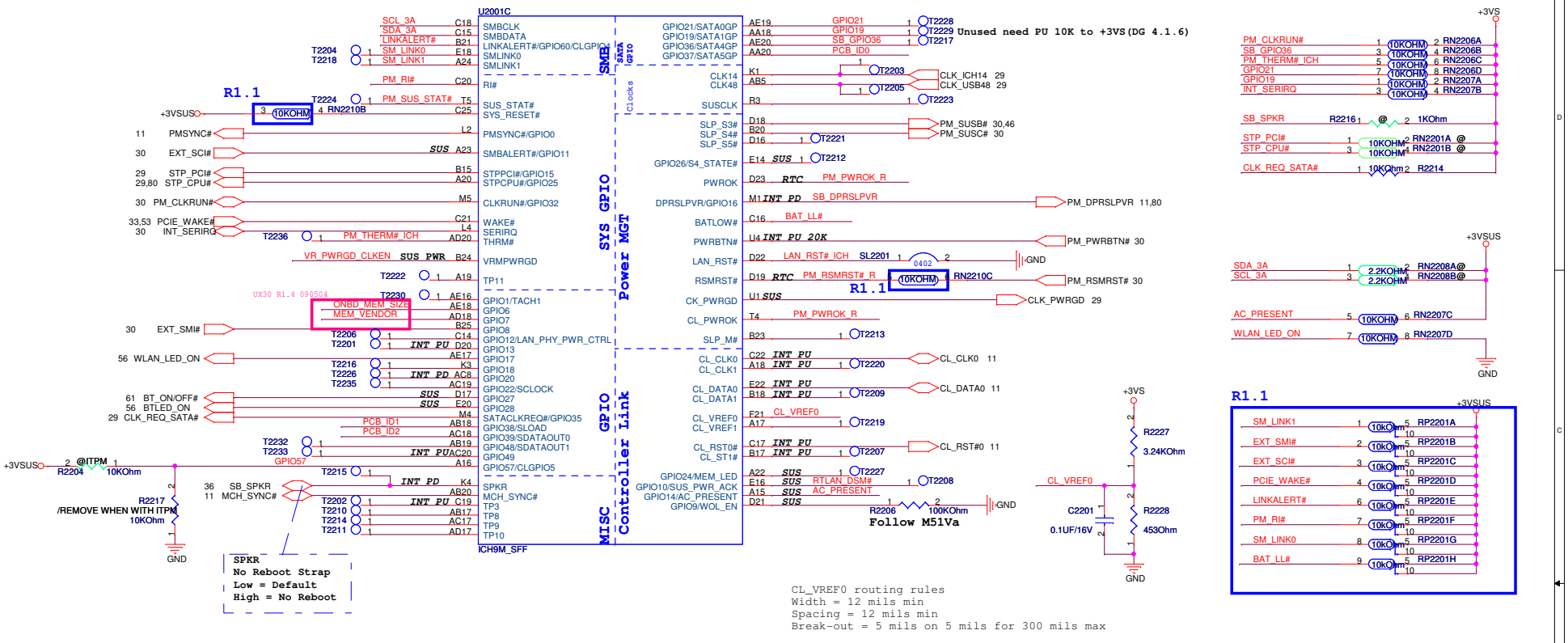
ASUS ASUSTeK COMPUTER INC

Title : ~~SB ICH9M PCI PCIE DMI USB~~

Engineer: *Uei Lee & Hacken*

Size	Project Name	Rev
Custom	UX30 MB	1.4

Date: Friday, May 08, 2009 Sheet 21 of 93



PCB ID	GPIO37 PCB_ID0	GPIO38 PCB_ID1	GPIO39 PCB_ID2
MBR1.0	0	0	0
MBR1.1	0	0	1
MBR1.3	0	1	0
MBR1.4	0	1	1
MBR2.0	1	0	0

UX30 R1.4 090504

GPIO 6	Memory Size
1	1GB
0	2GB

UX30 R1.4 090504

GPIO 7	Memory Vendor
1	SAMSUNG
0	NANYA

<Variant Name>

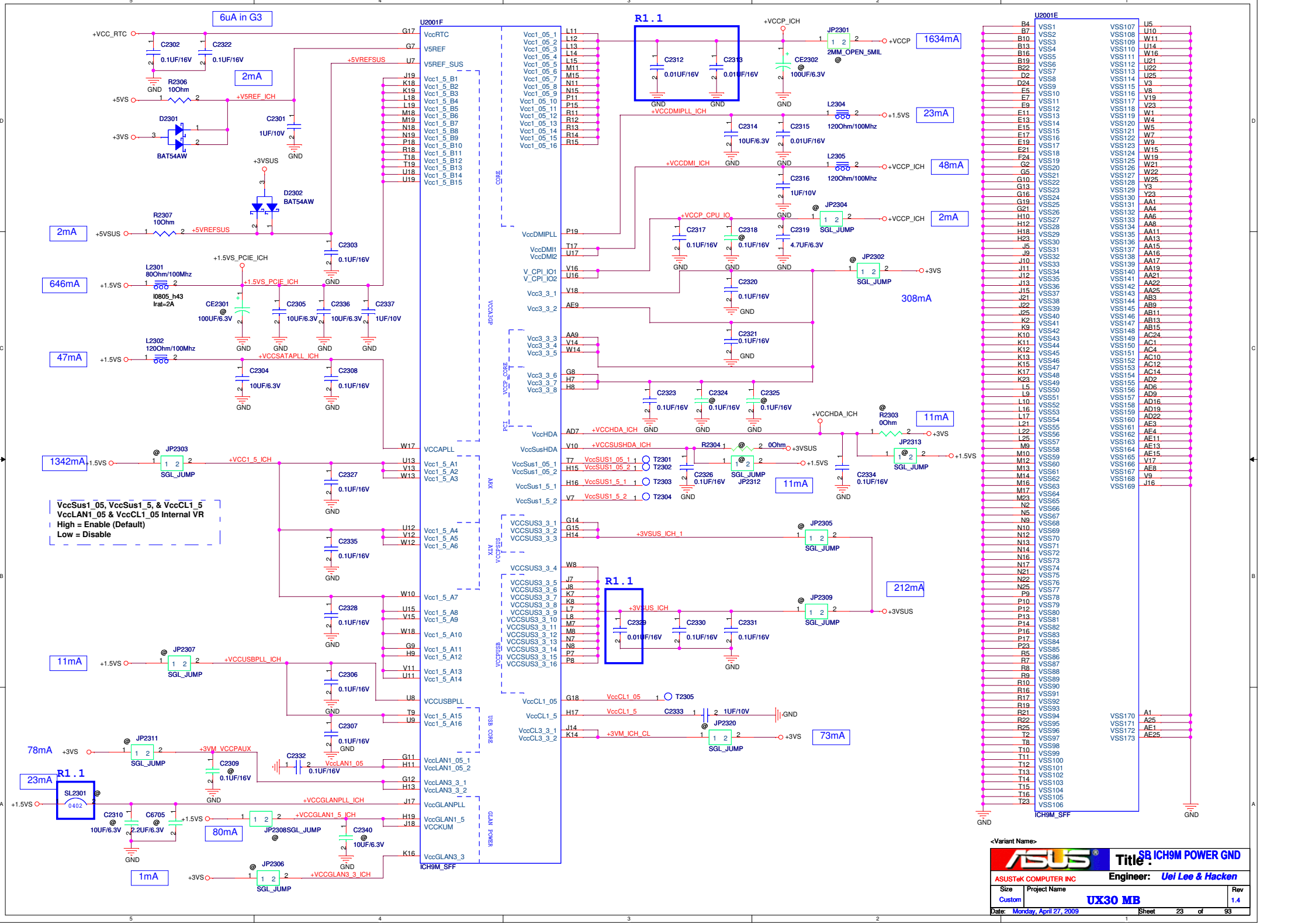
ASUSTeK COMPUTER INC

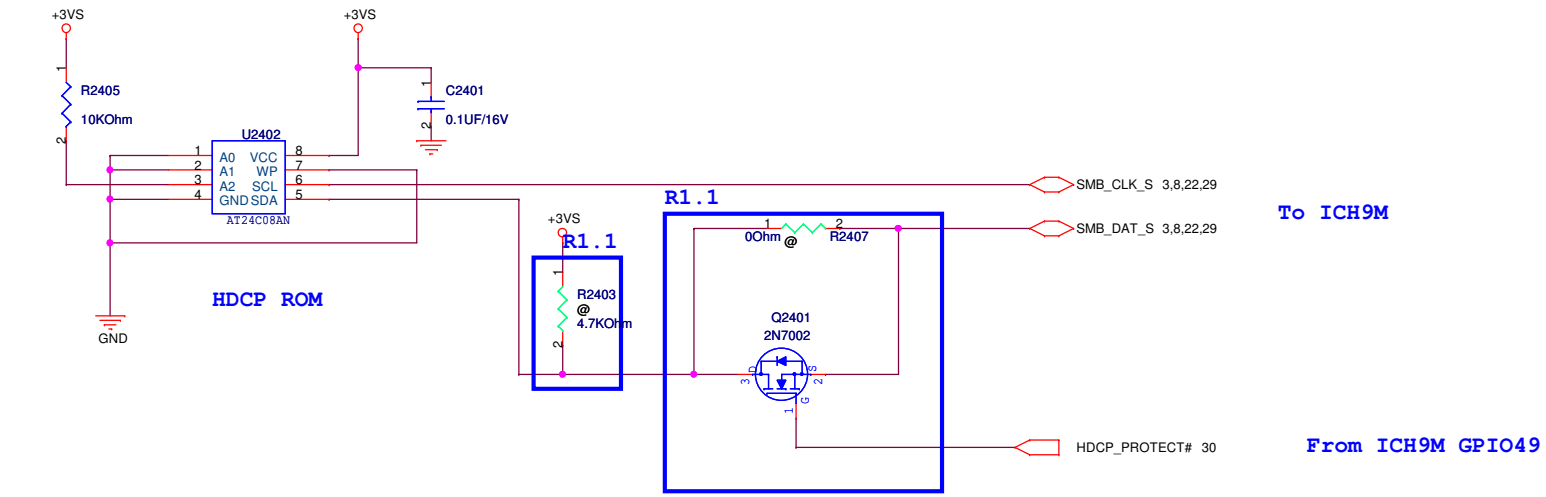
Title: SB ICH9M GPIO PMGT

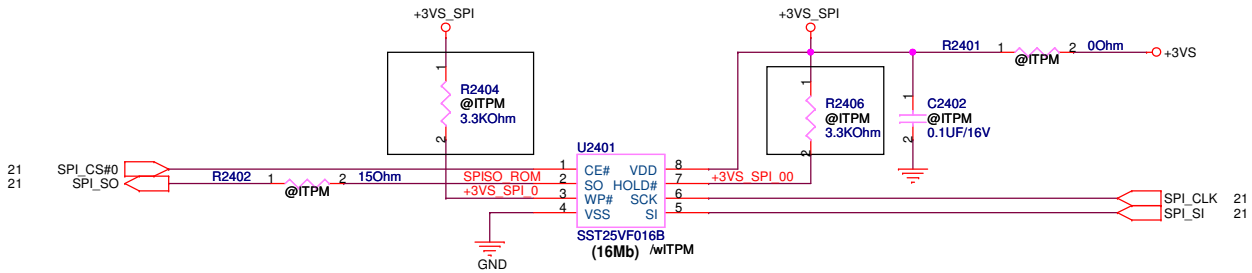
Engineer: Uei Lee & Hacken

Size	Project Name	Rev
Custom	UX30 MB	1.4

Date: Friday, May 08, 2009 Sheet 22 of 93


6uA in G3
U2001F
ICH9M_SFF
U2001E
ICH9M_SFF
R1.1
VccSus1_05, VccSus1_5, & VccCL1_5
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
1634mA
23mA
48mA
2mA
308mA
11mA
212mA
73mA
646mA
47mA
1342mA
78mA
80mA
1mA
<Variant Name>
Title : SB ICH9M POWER GND
ASUSTeK COMPUTER INC
Engineer: Uei Lee & Hacken
Size Custom
Project Name UX30 MB
Rev 1.4
Date: Monday, April 27, 2009
Sheet 23 of 93





FOR iTPM

<Variant Name>

ASUSTeK COMPUTER INC	Title : SB ICH9M SPI ROM & HDCP
	Engineer: Uei Lee & Hacken
Size B	Project Name UX30 MB
	Rev 1.4
Date: Friday, May 08, 2009	Sheet 24 of 93

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 25 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 26 of 93	

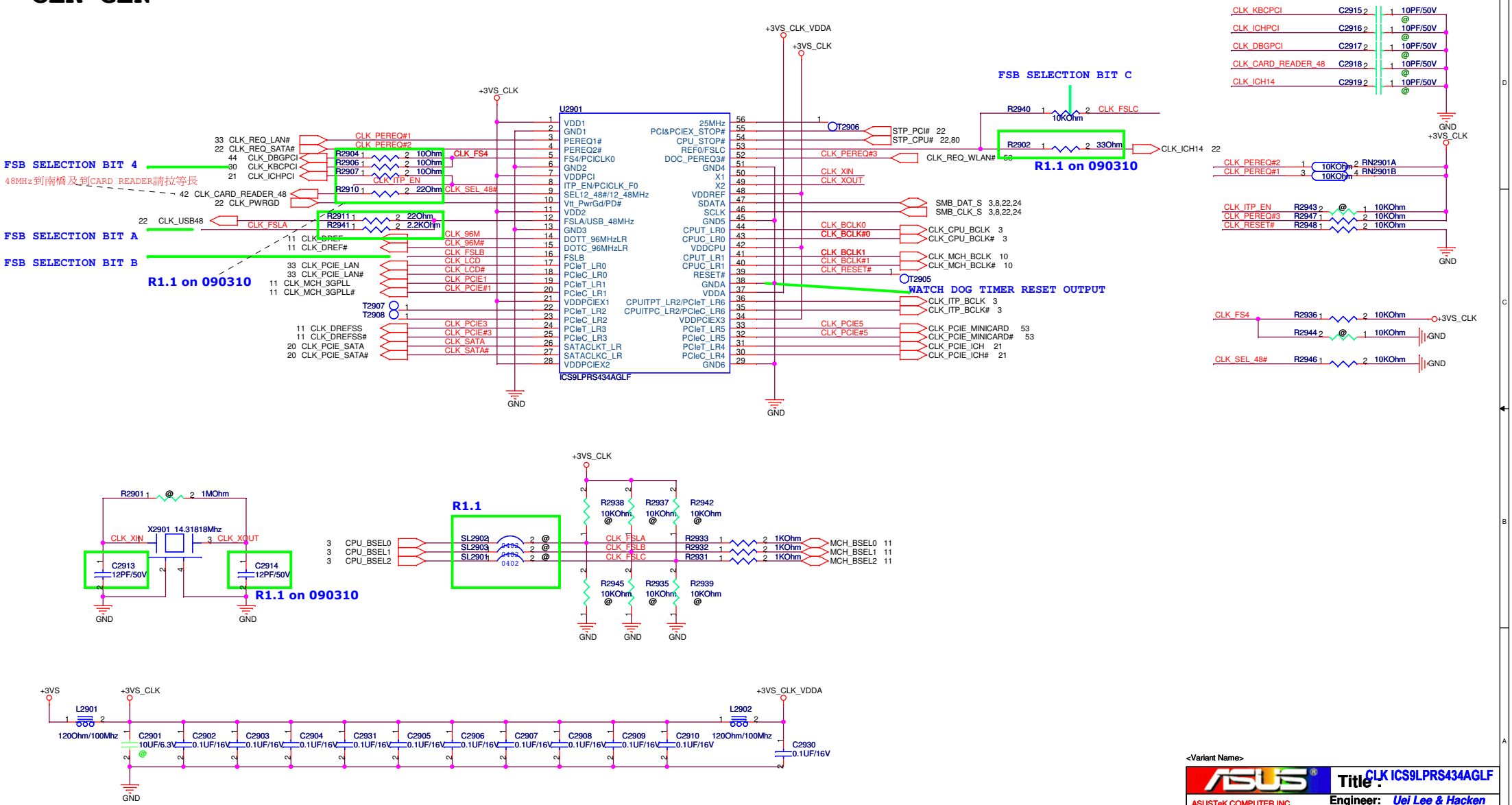
<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 27 of 93	

<Variant Name>

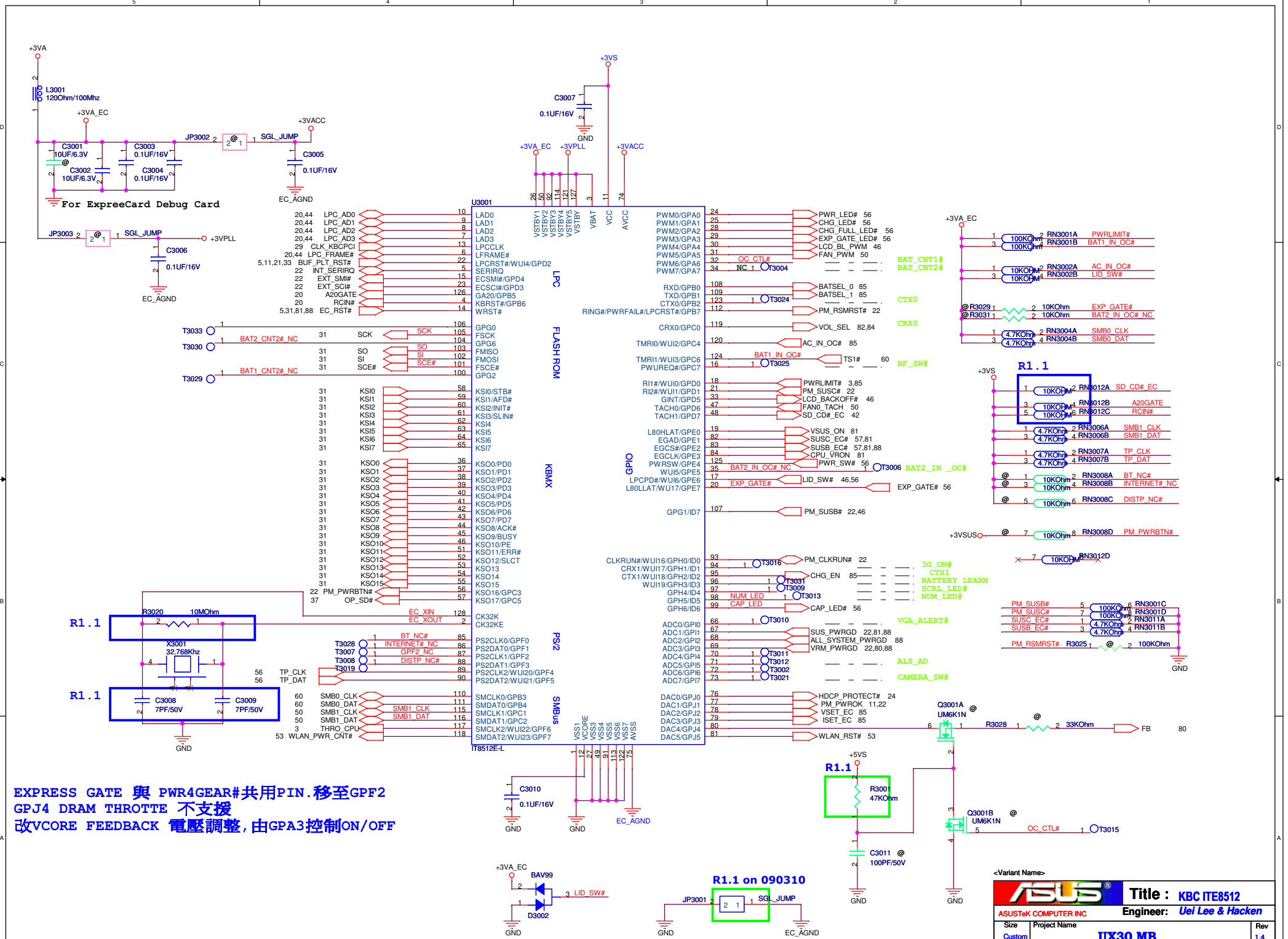
ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 28 of 93	

CLK GEN



<Variant Name>

ASUSTeK COMPUTER INC	Title : CLK ICS9LPRS434AGLF		
	Engineer: Uei Lee & Hacken		
Size: Custom	Project Name: UX30 MB		Rev: 1.4
Date: Friday, May 08, 2009	Sheet 29 of 93		


U3001
IT8512E-L
LPC
FLASH ROM
KBMX
PS/2
SMBus
GPIO
For ExpreeCard Debug Card
R1.1
R1.1 on 090310
EXPRESS GATE 與 PWR4GEAR#共用PIN.移至GPF2
GPJ4 DRAM THROTTE 不支援
改VCORE FEEDBACK 電壓調整,由GPA3控制ON/OFF
Title : KBC ITE8512
Engineer: Uei Lee & Hacken
ASUSTeK COMPUTER INC
Size Custom
Project Name UX30 MB
Rev 1.4
Date: Friday, May 08, 2009
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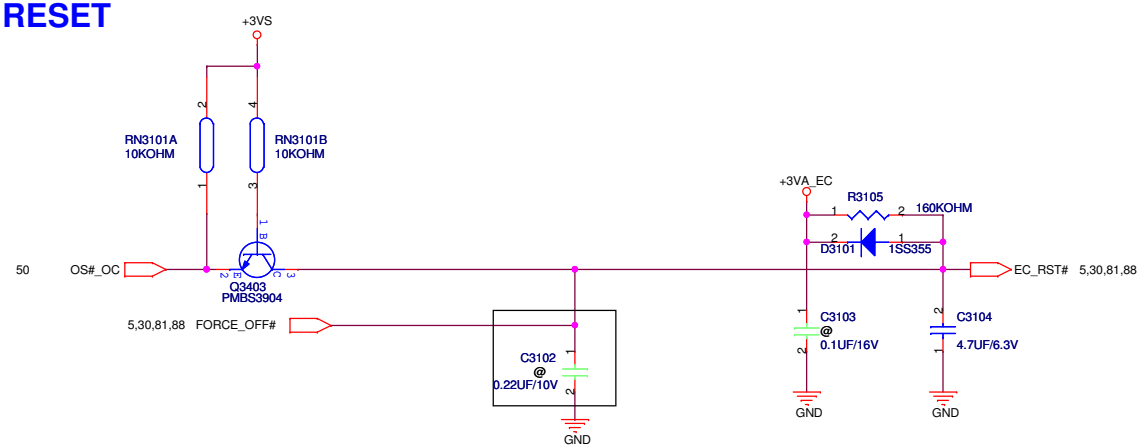
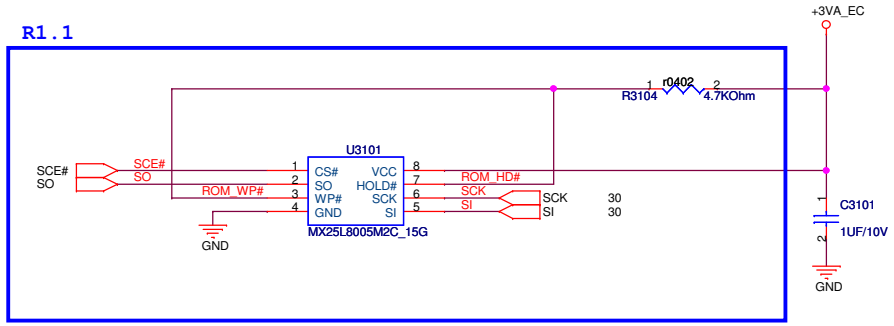
EC RESET



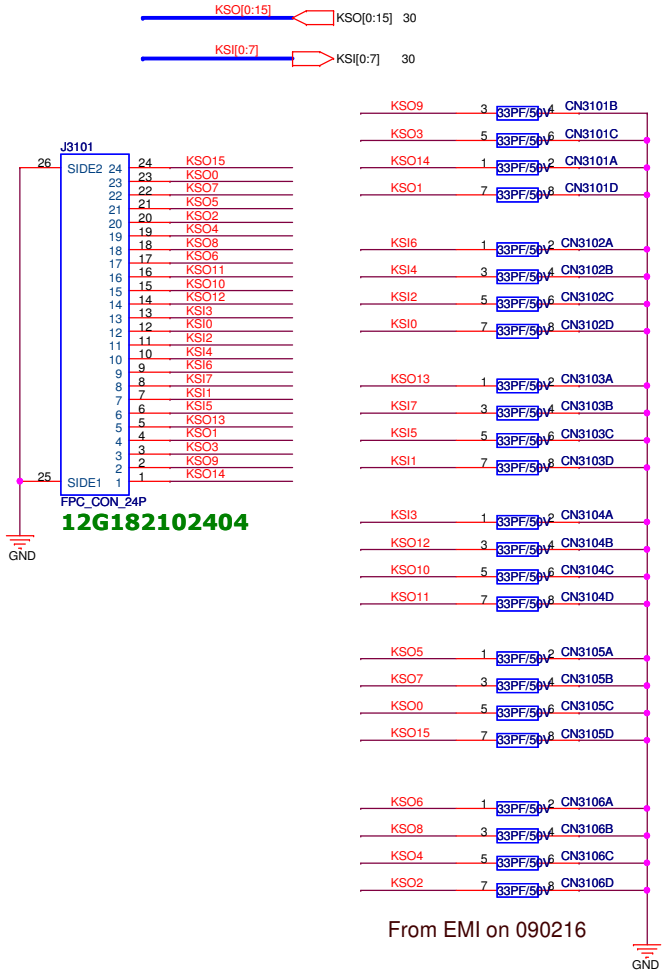
HALL SENSOR

R1.1 on 090310

8Mb SPI ROM



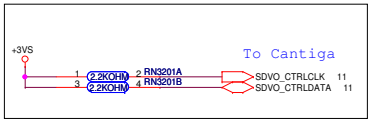
Internal Keyboard

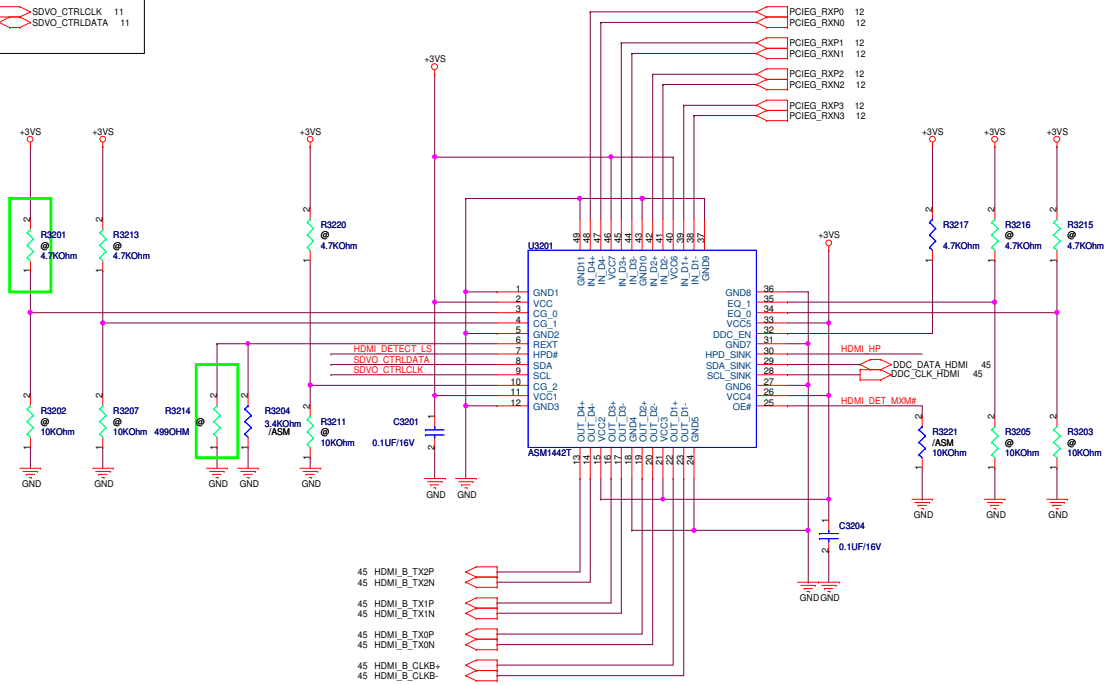


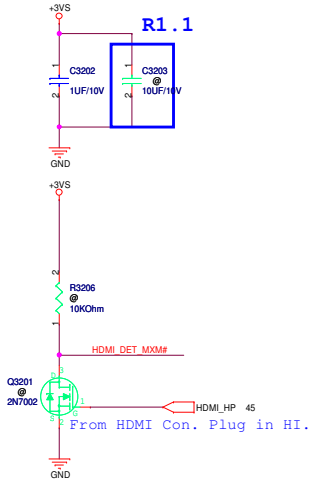
<Variant Name> ROM FLASH ROM TOUCH PAD KB

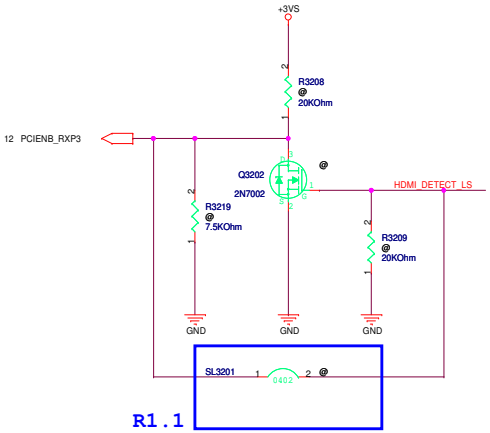
ASUS	Title :	
ASUSTeK COMPUTER INC	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 31 of 93	

UMA LEVEL SHIFTERS



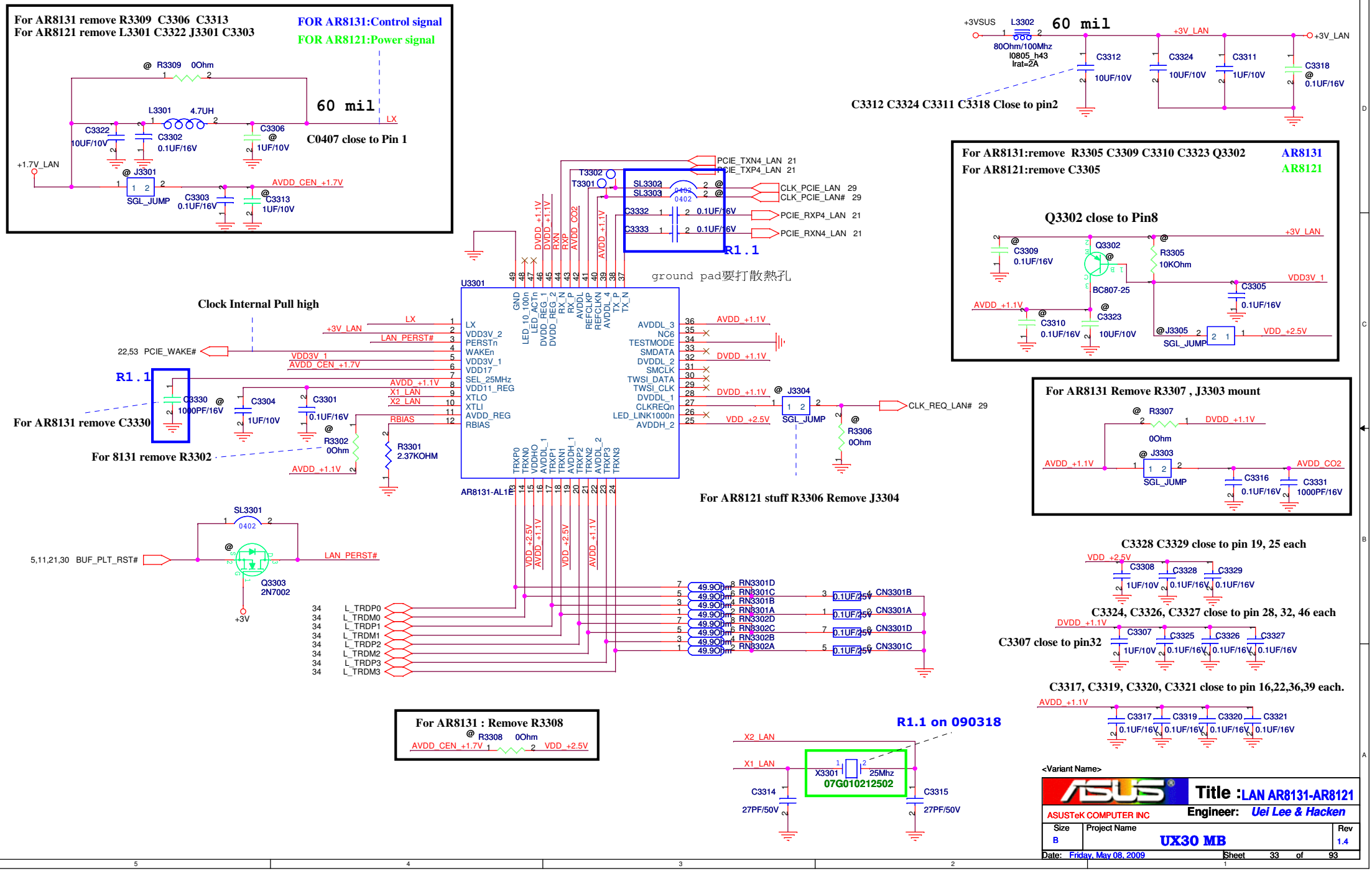


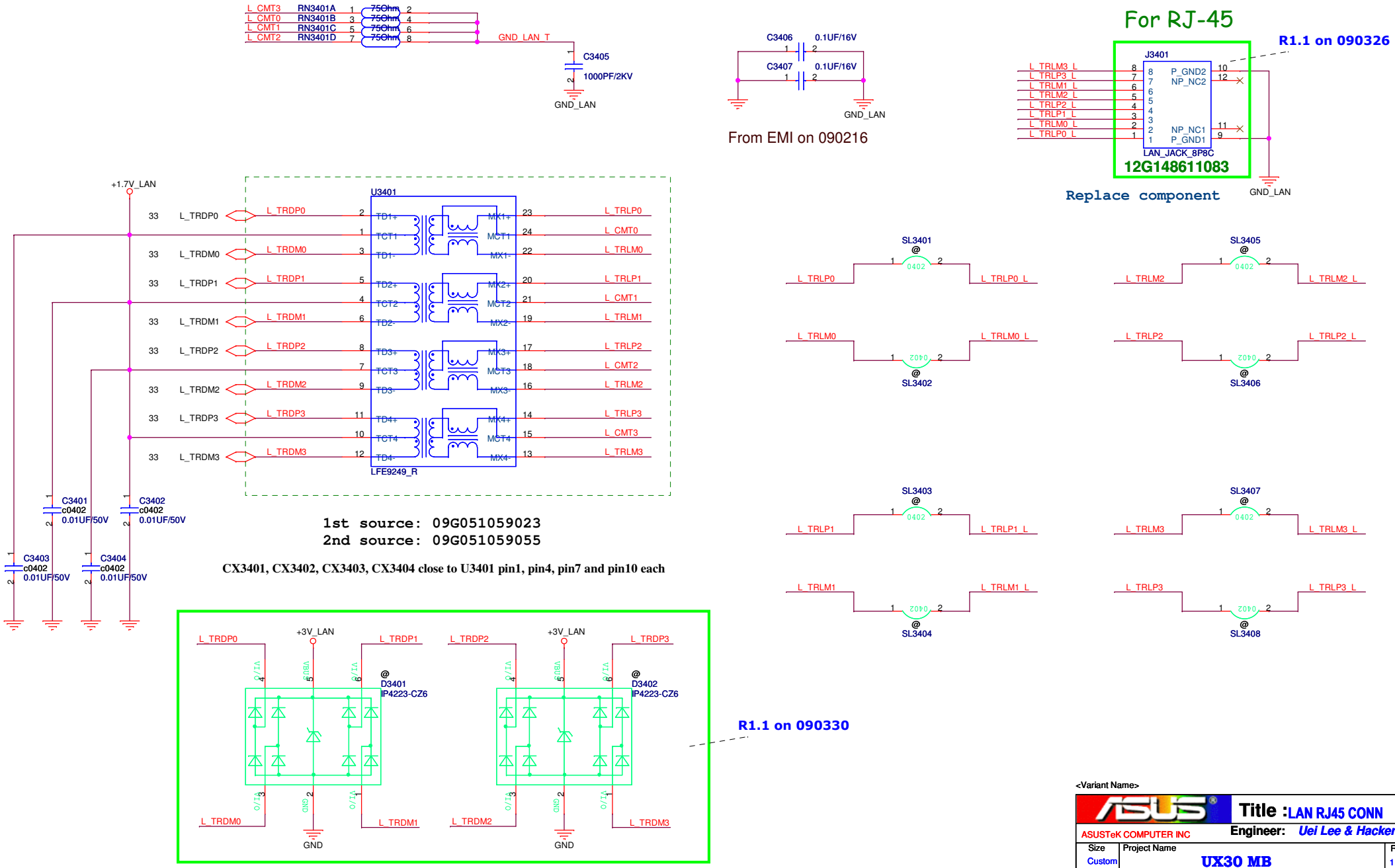




ASMedia ASM1442T
REMOVE:
R3201, R3214
MOUNT:
R3204,R3221

Parade PS8101T P/N:02G123000400
REMOVE:
R3204, R3221
MOUNT:
R3201, R3214
綠色外框的零件是上PS8101T要補上的零件
/ASM ASM1442T才要上的零件.上PS8101T時請移除


For AR8131 remove R3309 C3306 C3313
For AR8121 remove L3301 C3322 J3301 C3303
FOR AR8131:Control signal
FOR AR8121:Power signal
@ R3309 0Ohm
60 mil
L3301 4.7UH
C3322 10UF/10V
C3302 0.1UF/16V
C3306 @ 1UF/10V
LX
C0407 close to Pin 1
+1.7V_LAN
@ J3301
SGL_JUMP
C3303 0.1UF/16V
C3313 1UF/10V
AVDD_CEN_+1.7V
+3VSUS
L3302
80Ohm/100Mhz
l0805_h43
Irat=2A
60 mil
+3V_LAN
C3312 10UF/10V
C3324 10UF/10V
C3311 1UF/10V
C3318 @ 0.1UF/16V
C3312 C3324 C3311 C3318 Close to pin2
For AR8131:remove R3305 C3309 C3310 C3323 Q3302
For AR8121:remove C3305
AR8131
AR8121
Q3302 close to Pin8
C3309 0.1UF/16V
Q3302
BC807-25
R3305 10KOhm
VDD3V_1
C3305 0.1UF/16V
AVDD_+1.1V
C3310 0.1UF/16V
C3323 10UF/10V
@J3305
SGL_JUMP
VDD_+2.5V
PCIE_TXN4_LAN 21
PCIE_TXP4_LAN 21
T3302
T3301
SL3302
SL3303
CLK_PCIE_LAN 29
CLK_PCIE_LAN# 29
C3332 0.1UF/16V
C3333 0.1UF/16V
PCIE_RXP4_LAN 21
PCIE_RXN4_LAN 21
R1.1
ground pad要打散熱孔
U3301
AR8131-AL1B
Clock Internal Pull high
22,53 PCIE_WAKE#
+3V_LAN
LX
LAN_PERST#
VDD3V_1
AVDD_CEN_+1.7V
AVDD_+1.1V
X1_LAN
X2_LAN
RBIAS
R1.1
C3330 @ 1000PF/16V
For AR8131 remove C3330
C3304 1UF/10V
C3301 0.1UF/16V
R3302 0Ohm
R3301 2.37KOHM
For 8131 remove R3302
AVDD_+1.1V
DVDD_+1.1V
VDD_+2.5V
@ J3304
SGL_JUMP
CLK_REQ_LAN# 29
R3306 0Ohm
For AR8121 stuff R3306 Remove J3304
For AR8131 Remove R3307 , J3303 mount
@ R3307
0Ohm
DVDD_+1.1V
AVDD_+1.1V
@ J3303
SGL_JUMP
C3316 0.1UF/16V
C3331 1000PF/16V
AVDD_CO2
SL3301
0402
5,11,21,30 BUF_PLT_RST#
LAN_PERST#
Q3303 2N7002
+3V
L_TRDP0
L_TRDM0
L_TRDP1
L_TRDM1
L_TRDP2
L_TRDM2
L_TRDP3
L_TRDM3
RN3301D
RN3301C
RN3301B
RN3301A
RN3302D
RN3302C
RN3302B
RN3302A
CN3301B
CN3301A
CN3301D
CN3301C
0.1UF/25V
C3328 C3329 close to pin 19, 25 each
VDD_+2.5V
C3308 1UF/10V
C3328 0.1UF/16V
C3329 0.1UF/16V
C3324, C3326, C3327 close to pin 28, 32, 46 each
DVDD_+1.1V
C3307 close to pin32
C3307 1UF/10V
C3325 0.1UF/16V
C3326 0.1UF/16V
C3327 0.1UF/16V
C3317, C3319, C3320, C3321 close to pin 16,22,36,39 each.
AVDD_+1.1V
C3317 0.1UF/16V
C3319 0.1UF/16V
C3320 0.1UF/16V
C3321 0.1UF/16V
For AR8131 : Remove R3308
@ R3308 0Ohm
AVDD_CEN_+1.7V
VDD_+2.5V
R1.1 on 090318
X2_LAN
X1_LAN
X3301 25Mhz
07G010212502
C3314 27PF/50V
C3315 27PF/50V
<Variant Name>
Title :LAN AR8131-AR8121
ASUSTeK COMPUTER INC
Engineer: Uei Lee & Hacken
Size B
Project Name UX30 MB
Rev 1.4
Date: Friday, May 08, 2009
Sheet 33 of 93

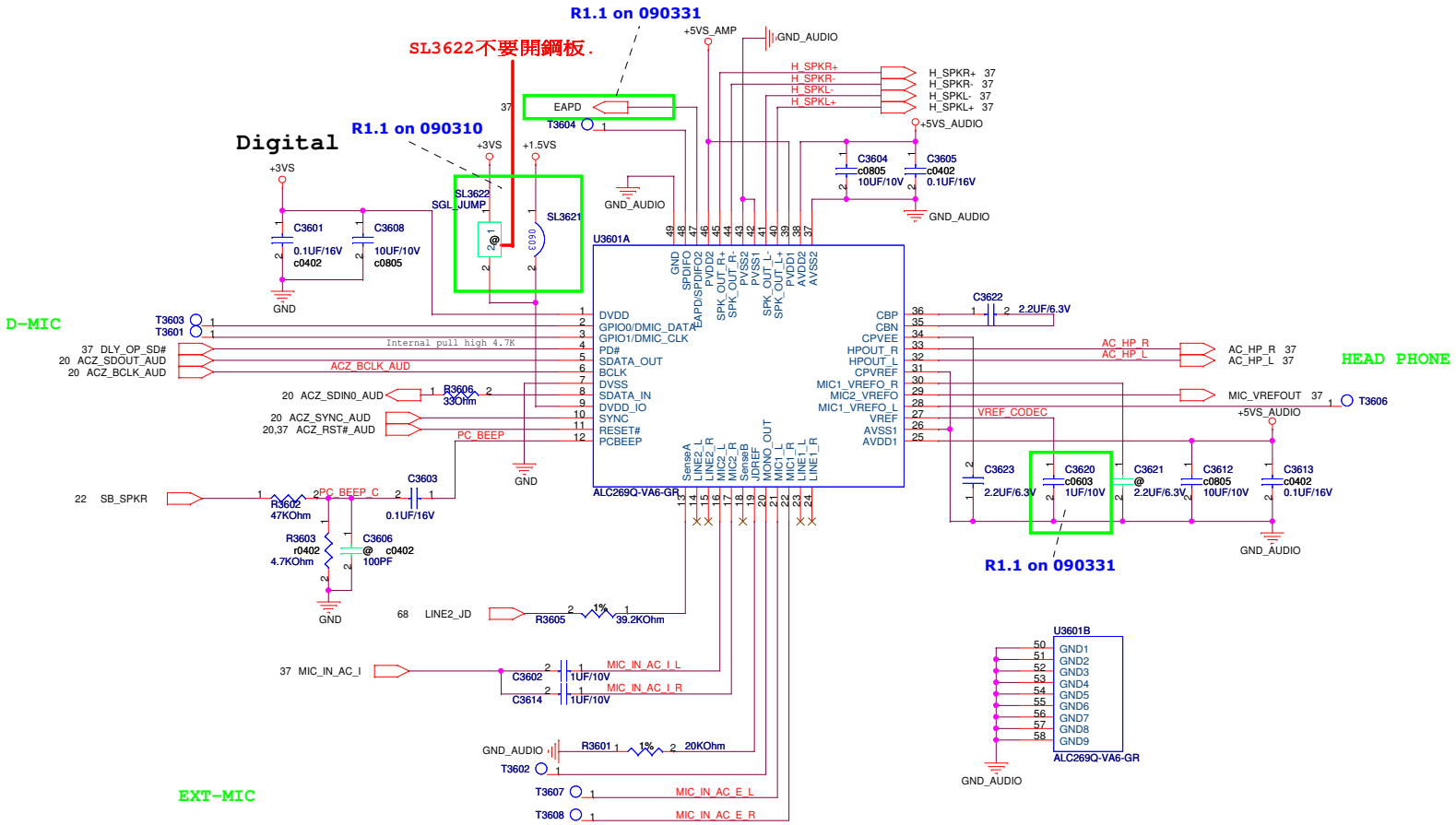


<Variant Name>

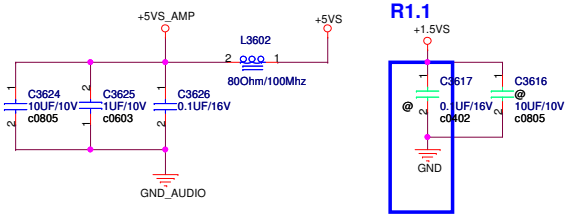
ASUSTeK COMPUTER INC	Title : LAN RJ45 CONN	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 34 of 93	

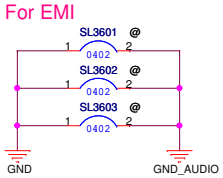
<Variant Name>

ASUSTeK COMPUTER INC	Title :	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 35 of 93	

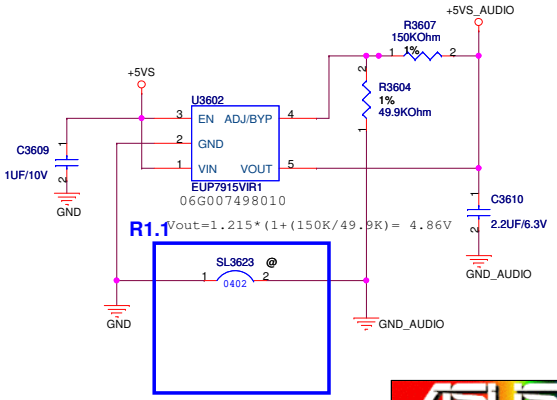


Input impedence:64K ohm(Typical)

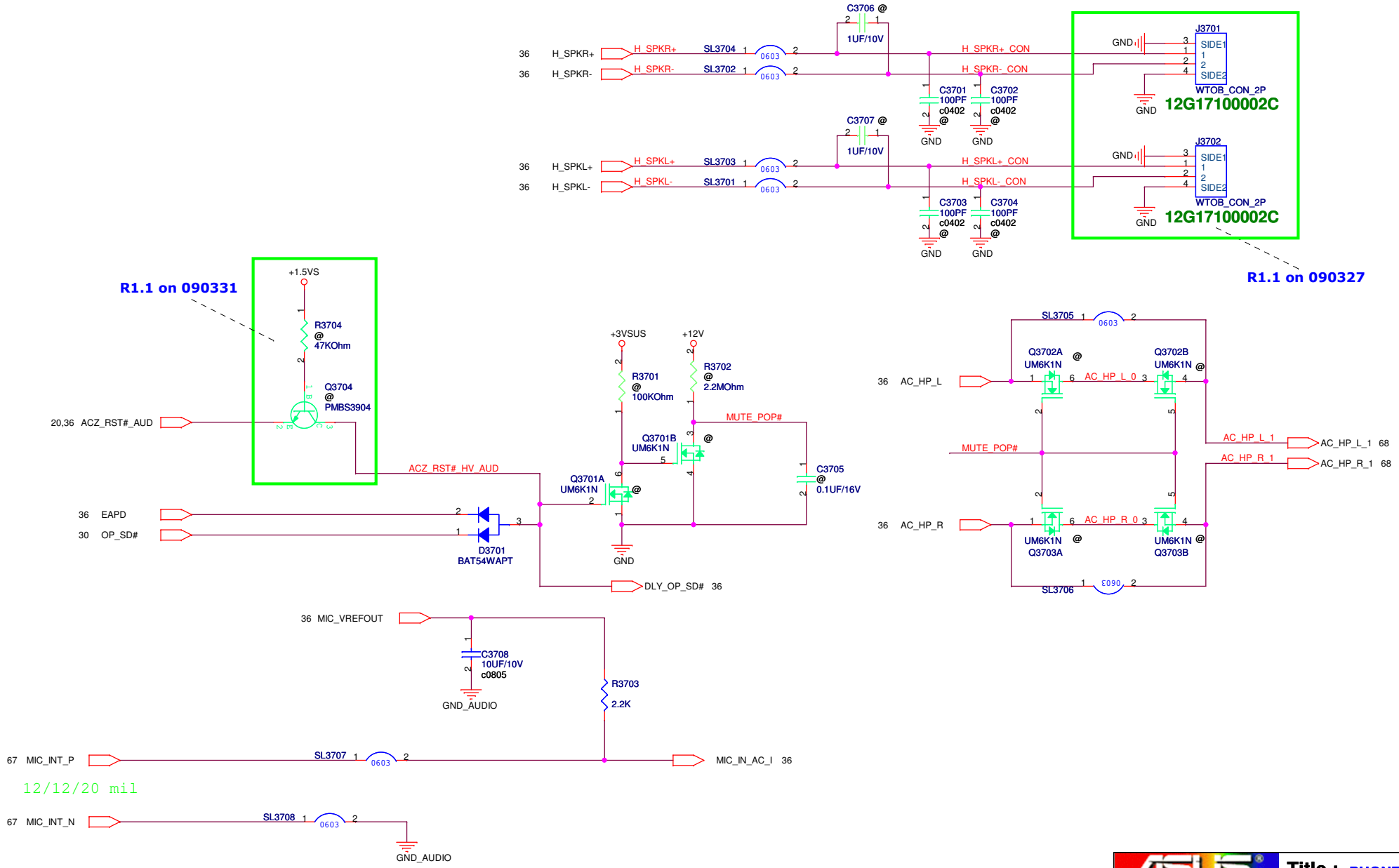




From EMI on 090201



ASUSTeK COMPUTER INC. NB1	Title : CODEC	Engineer:
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 36 of 93	



ASUSTeK COMPUTER INC. NB1	Title : PHONE JACK	
	Engineer:	
Size B	Project Name UX30 MB	Rev 1.4
Date: Friday, May 08, 2009	Sheet 37 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 38 of 93	

<Variant Name>

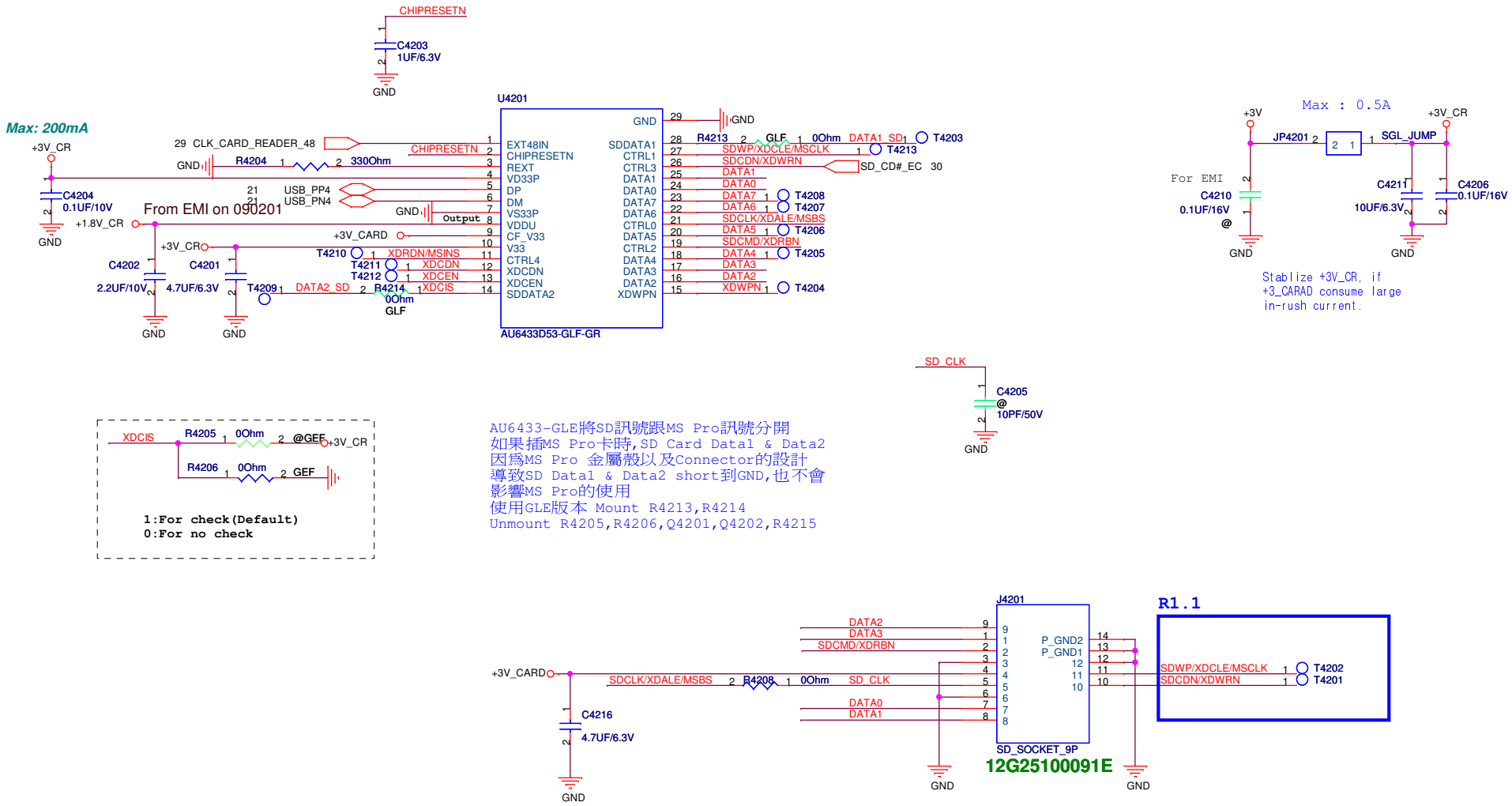
ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 39 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 40 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 41 of 93	



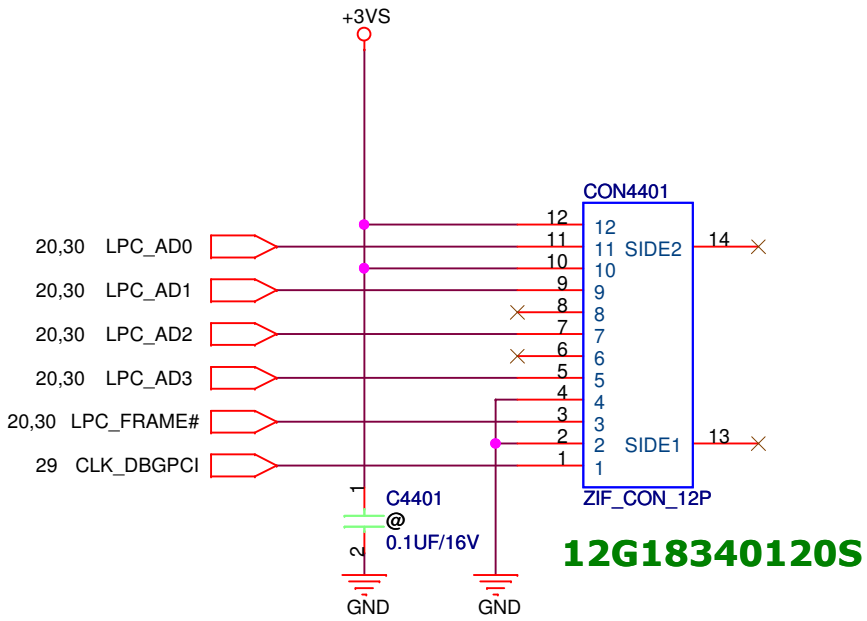
<Variant Name>

ASUSTeK COMPUTER INC	Title : CARD READER AU6433
	Engineer: Uei Lee & Hacken
Size: B	Project Name: UX30 MB
	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 42 of 93

<Variant Name>

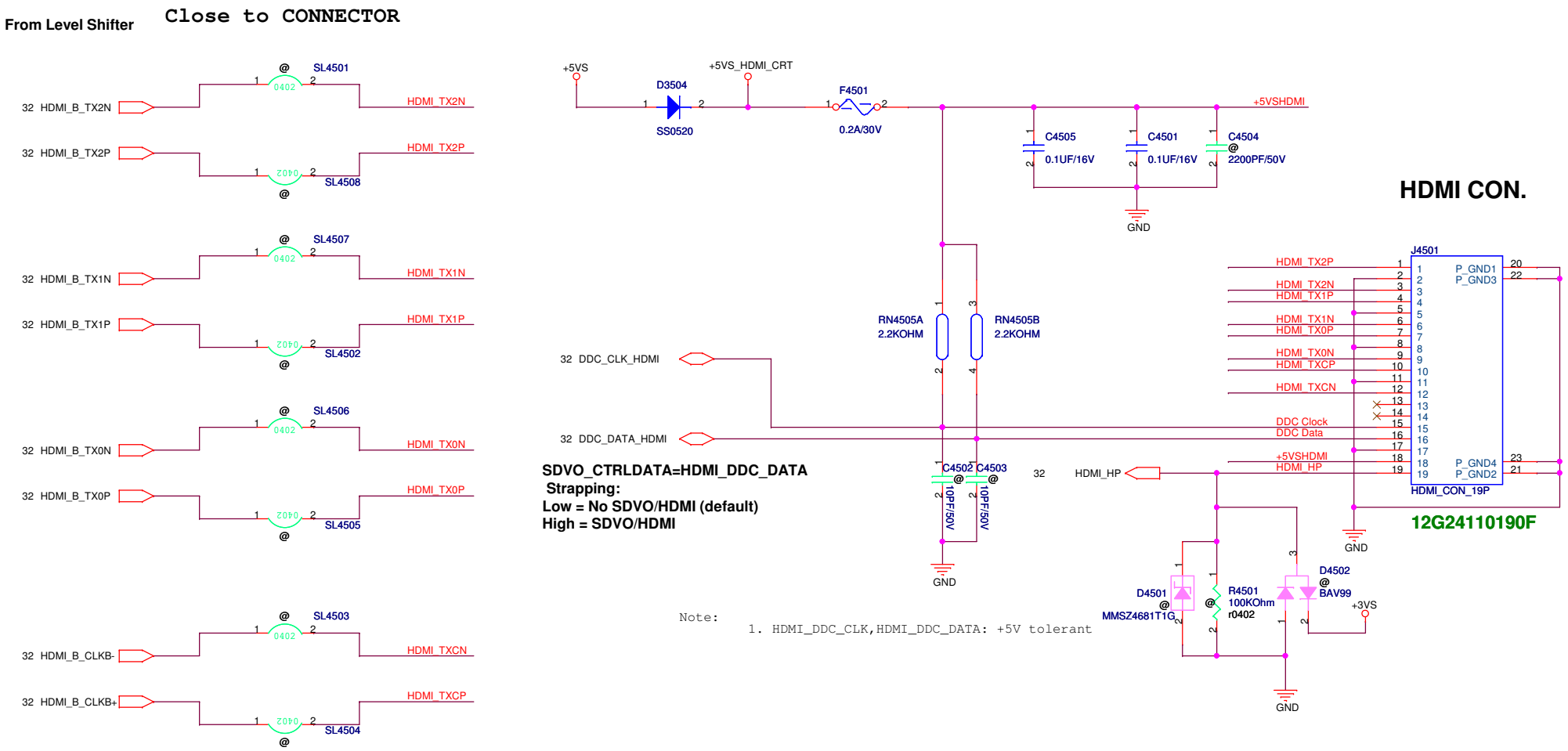
ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 43 of 93	

LPC DEBUG PORT



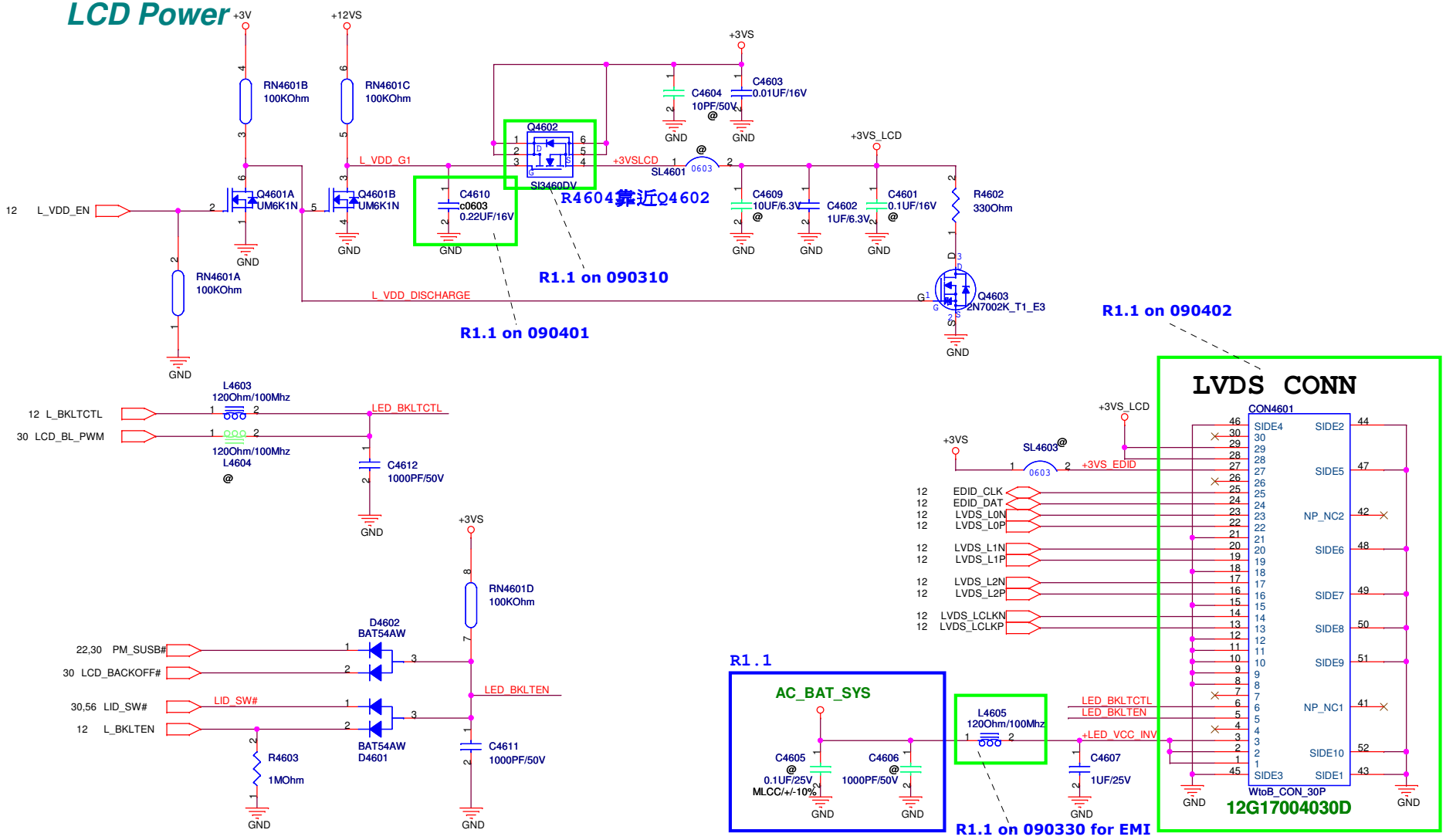
<Variant Name>

ASUSTeK COMPUTER INC	Title : BUG DEBUG PORT	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 44 of 93	



<Variant Name>

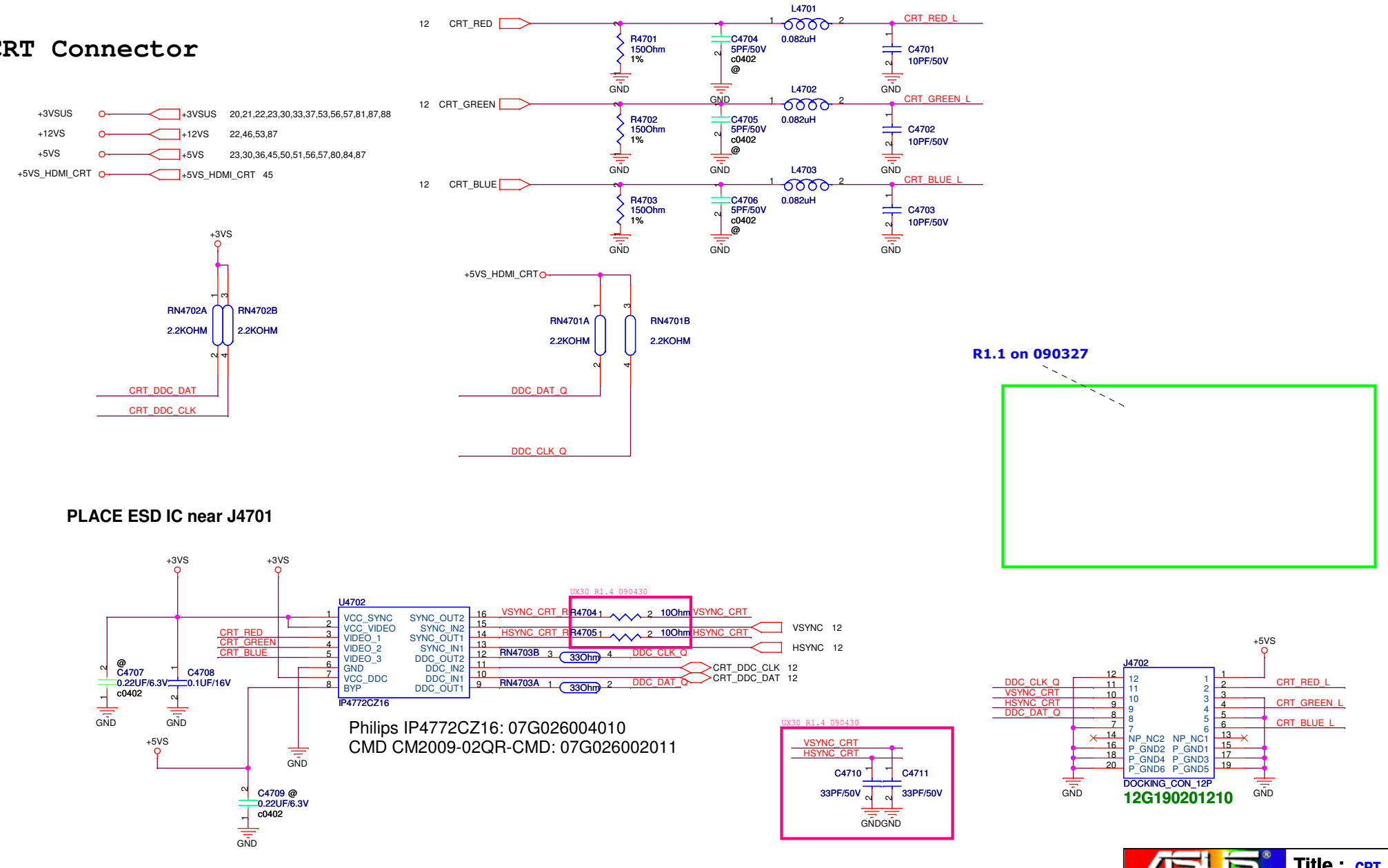
ASUSTeK COMPUTER INC	Title : HDMI CONN
	Engineer: Uei Lee & Hacken
Size: B	Project Name: UX30 MB
Rev: 1.4	
Date: Friday, May 08, 2009	Sheet 45 of 93



<Variant Name>

ASUSTeK COMPUTER INC	Title : CRT LVDS CONN	
	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 1.4
Date: Friday, May 08, 2009	Sheet 46 of 93	

CRT Connector



Title : CRT		
<OrgName>	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 1.4
Date: Friday, May 08, 2009	Sheet 47 of 93	

<Variant Name>

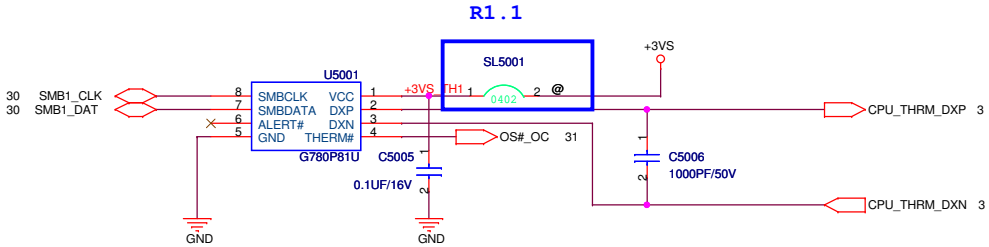
ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 48 of 93	

<Variant Name>

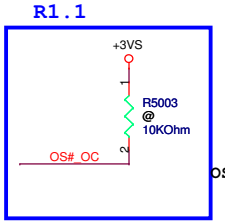
ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 49 of 93	

Thermal Seneor

CPU

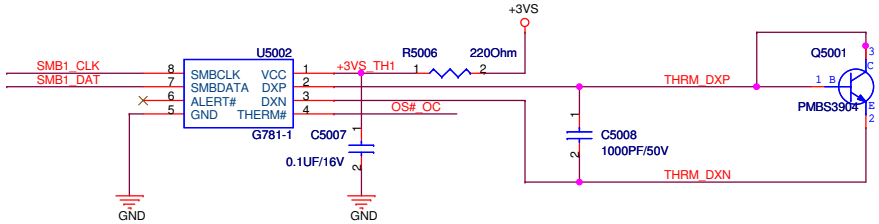


SMBus Address: G780 98H



OS#_OC PULL HIGH AT Page 31.

CHASSIS



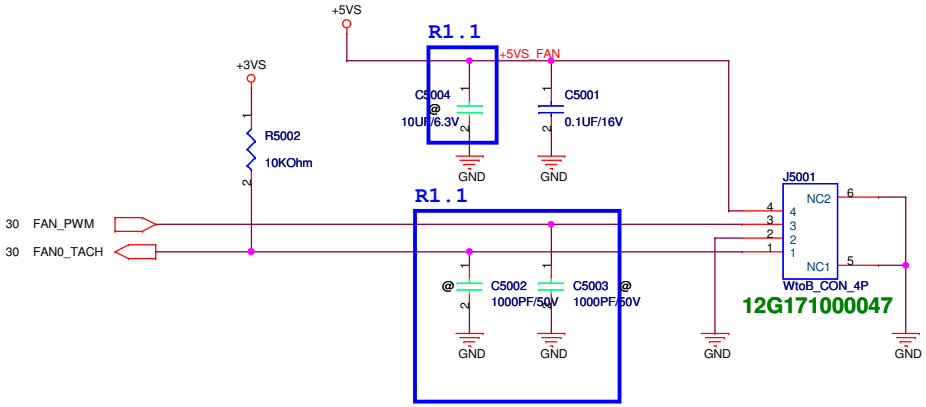
SMBus Address: G780 9AH

Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
10 mils
----------OTHER SIGNALS

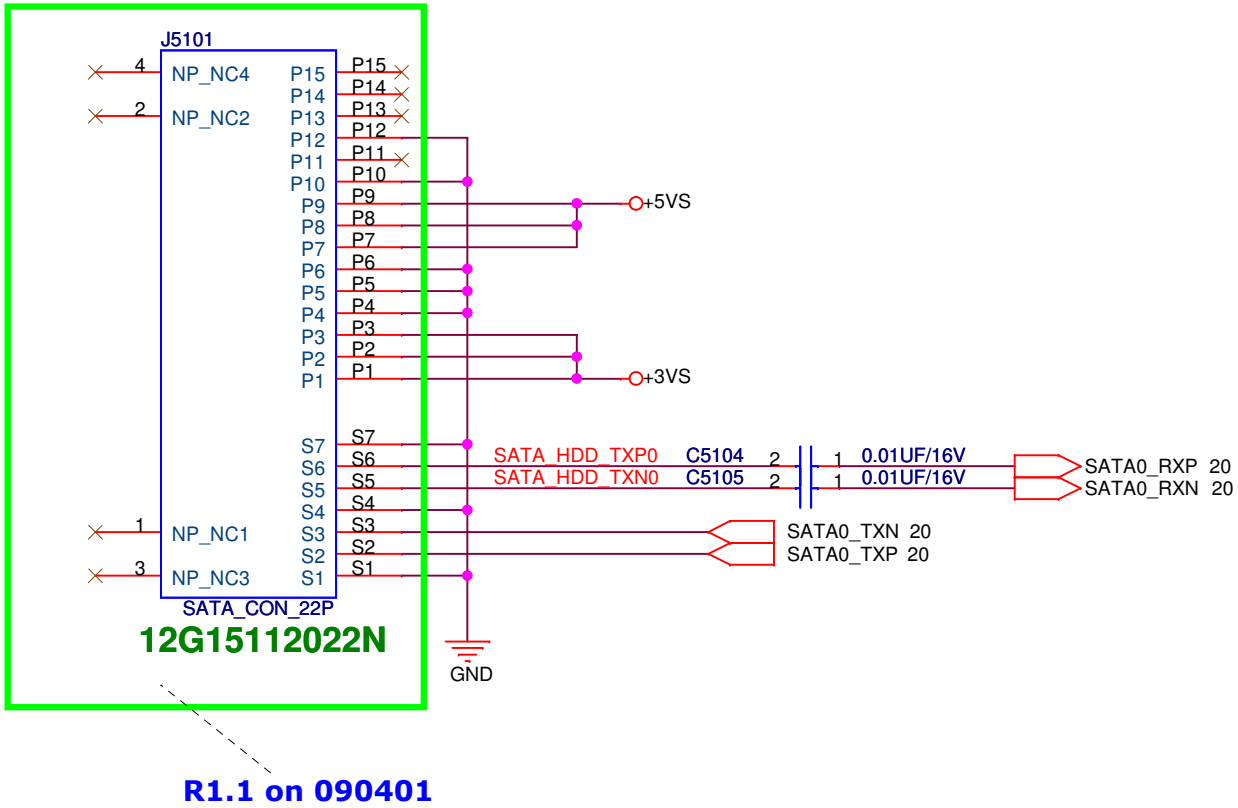
Avoid FSB,Power

FAN CONN

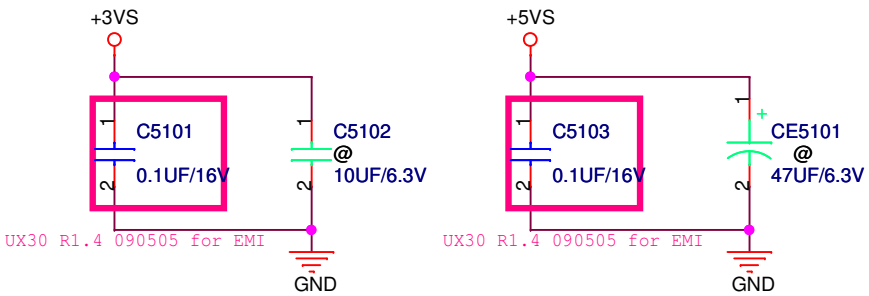


<Variant Name>

ASUSTeK COMPUTER INC	Title : FAN THERMAL SENSOR FAN CONN	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 50 of 93	

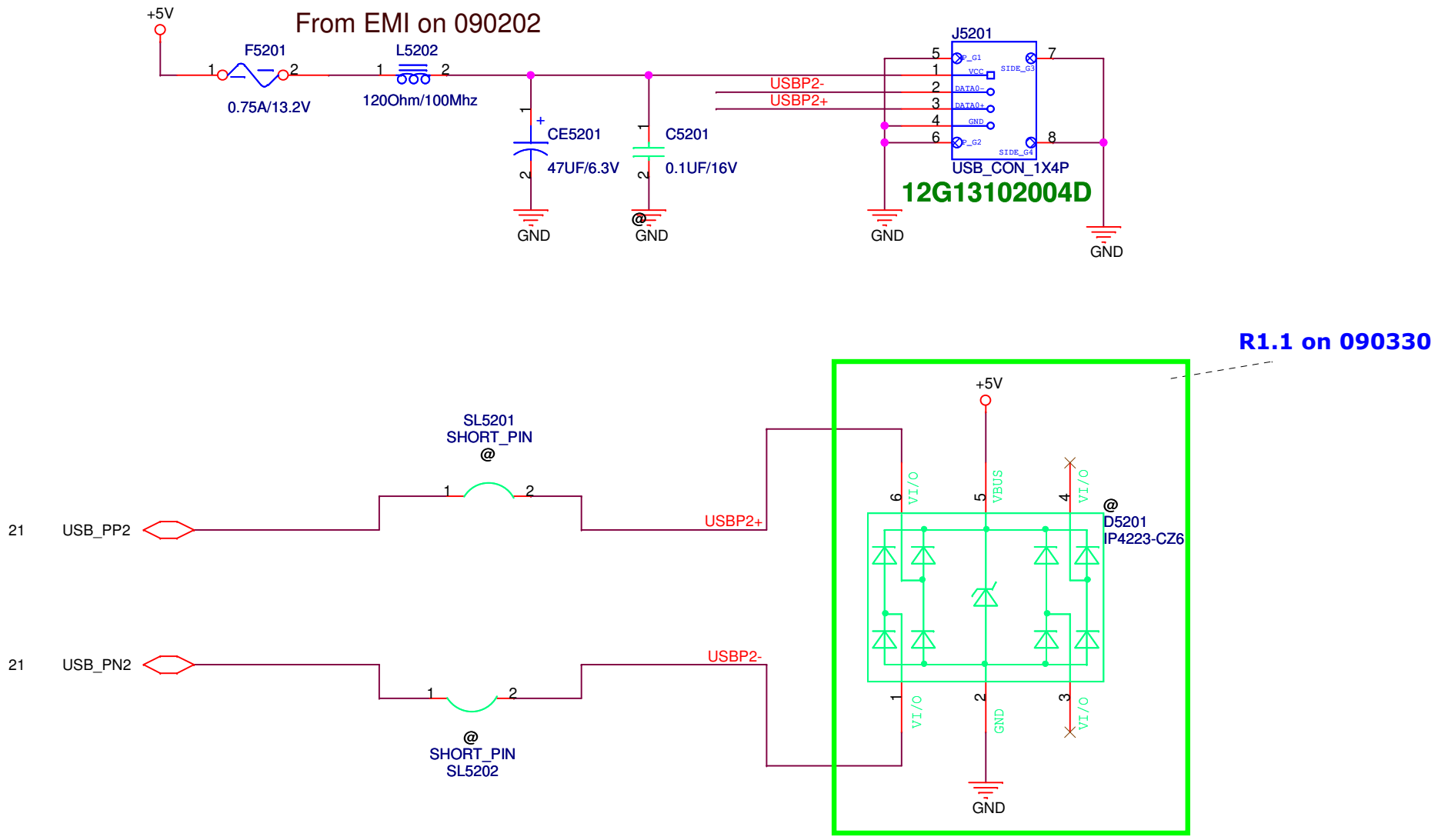


3VS 5VS 線寬拉80mils



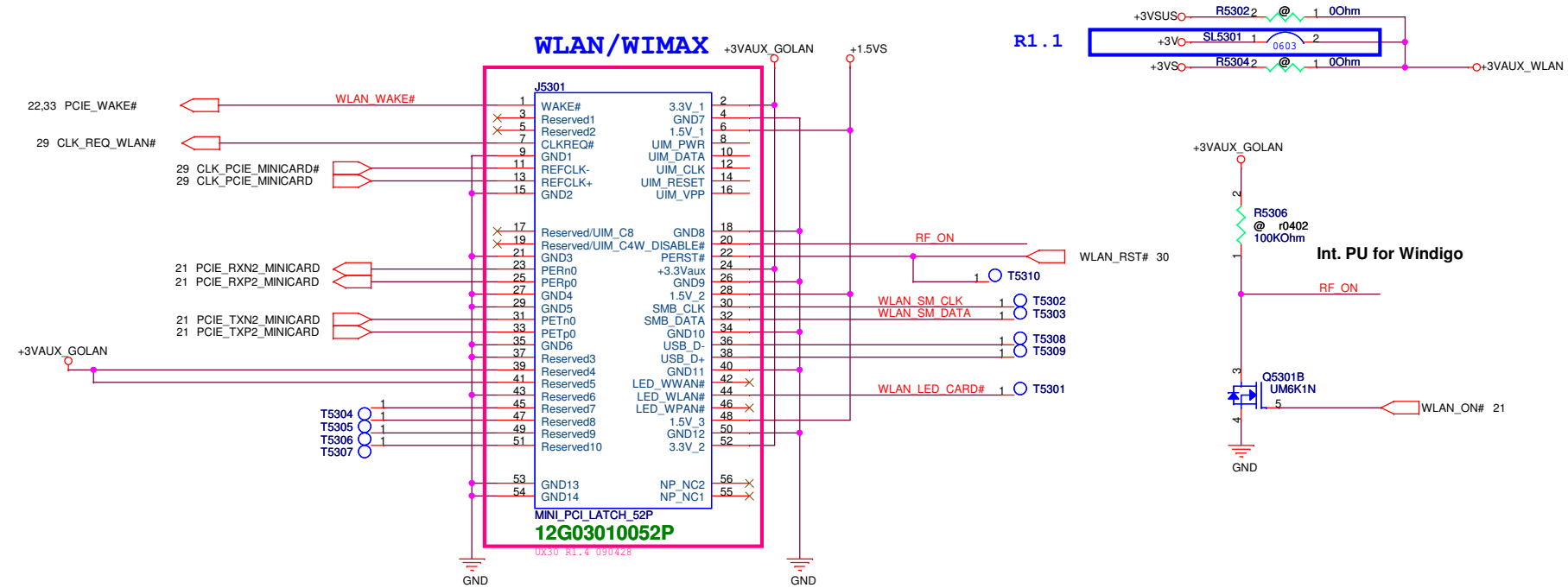
<Variant Name>

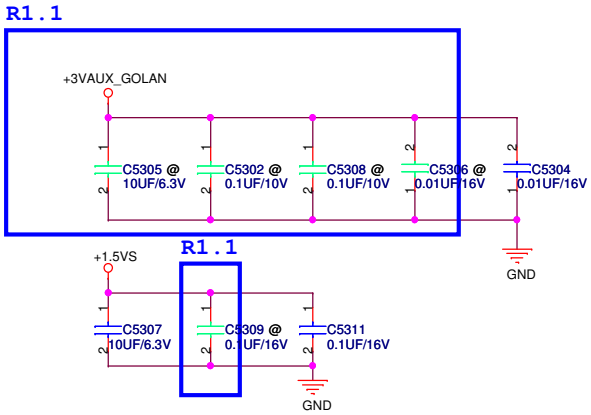
ASUSTeK COMPUTER INC	Title : XDD SATA HDD CONN	
	Engineer: Uei Lee & Hacken	
Size A	Project Name UX30 MB	Rev 1.4
Date: Friday, May 08, 2009	Sheet 51 of 93	

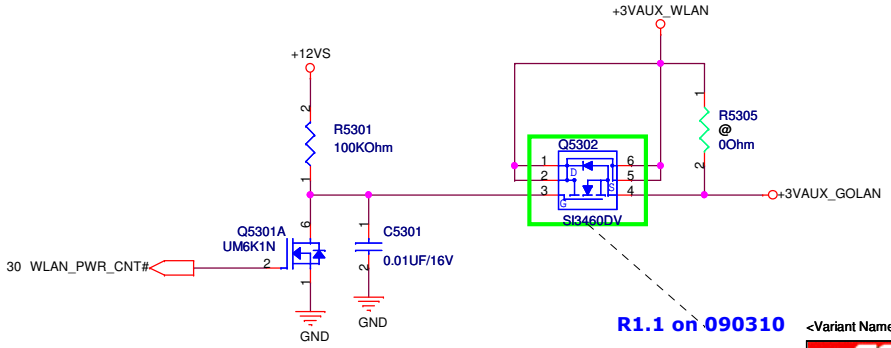


<Variant Name>

ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 52 of 93	







<Variant Name>

ASUSTeK COMPUTER INC	Title : PCI-E WLAN	
	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 1.4
Date: Friday, May 08, 2009	Sheet 53 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 54 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
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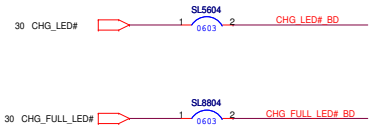
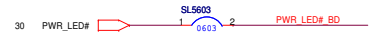
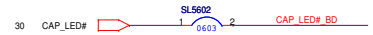
CHARGE LED



POWER LED



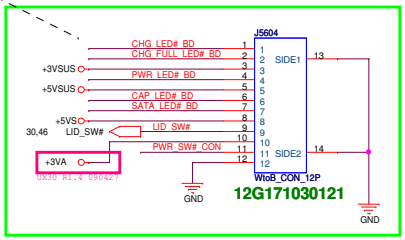
CAP LOCK LED



NUM LOCK LED

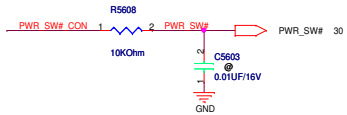
R1.1 on 090330

R1.1 on 090327



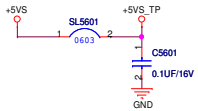
R1.1

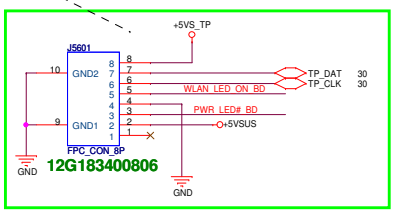
POWER BTN



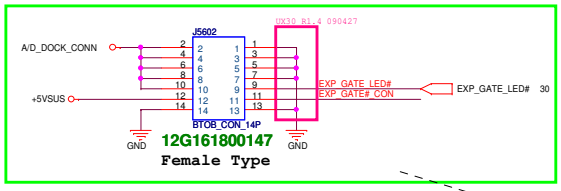
Touch-Pad

R1.1 on 090327

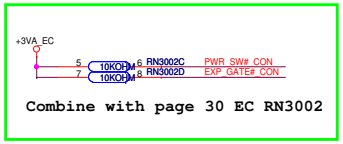




EXPRESS GATE BTN and DC-IN

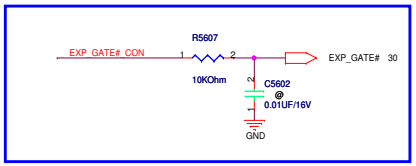


R1.1 on 090401

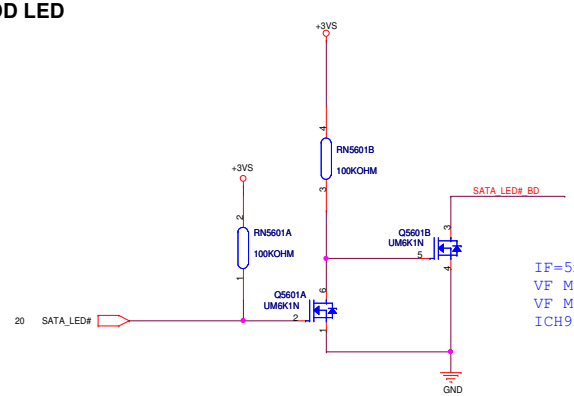


EXPRESS GATE BTN

R1.1

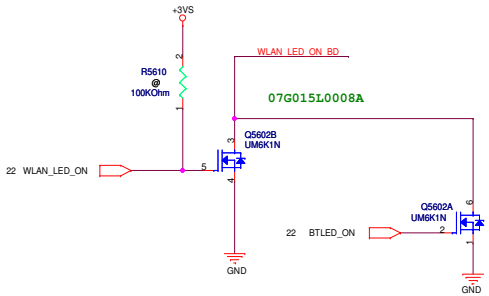


HDD LED



IF=5mA
VF Min. 2.55V
VF Max. 3.25V
ICH9 Sink Current Max 6mA

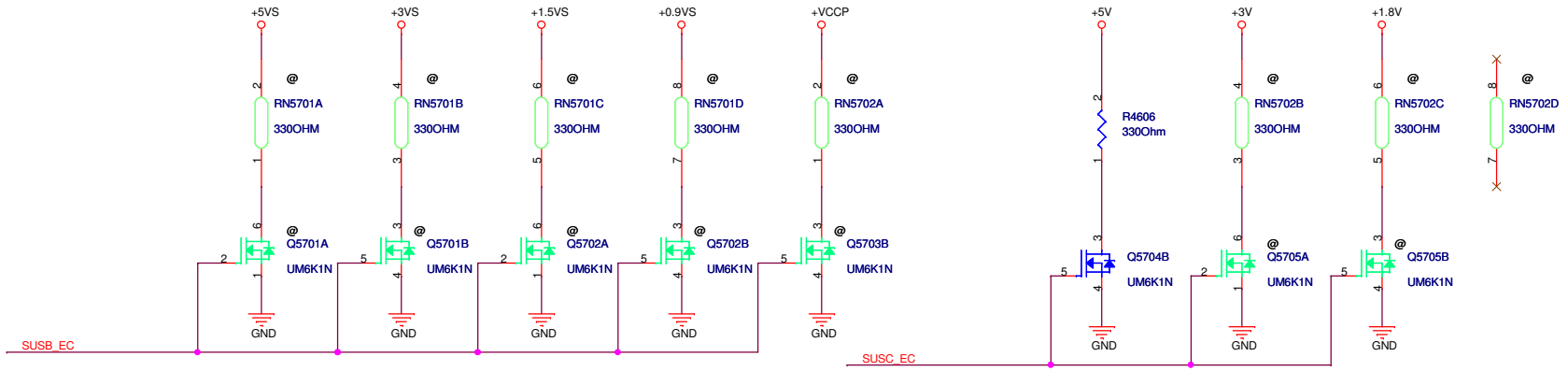
WireLess/BT LED

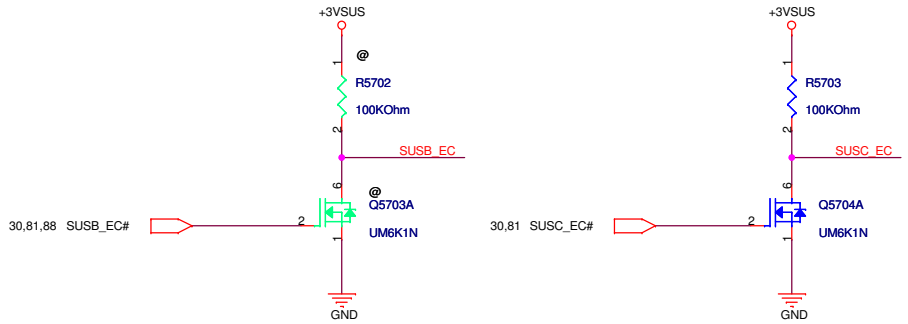


IF=5mA
VF Min. 2.55V
VF Max. 3.25V

Discharge Circuit

+5VS	+5VS	23,30,36,45,47,50,51,56,80,84,87
+3VS	+3VS	3,8,11,12,15,17,21,22,23,24,29,30,31,32,36,44,45,46,47,50,51,53,56,80,87,88
+1.5VS	+1.5VS	4,15,20,23,36,37,53,84
+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,82
+5V	+5V	52,68,87
+3V	+3V	21,33,42,46,53,61,67,87
+1.8V	+1.8V	8,9,11,14,19,83,87
+0.9VS	+0.9VS	9,83
+3VSUS	+3VSUS	20,21,22,23,30,33,37,53,56,81,87,88





<Variant Name>

ASUSTeK COMPUTER INC	Title : DSG DISCHARHE CIRCUIT	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 57 of 93	

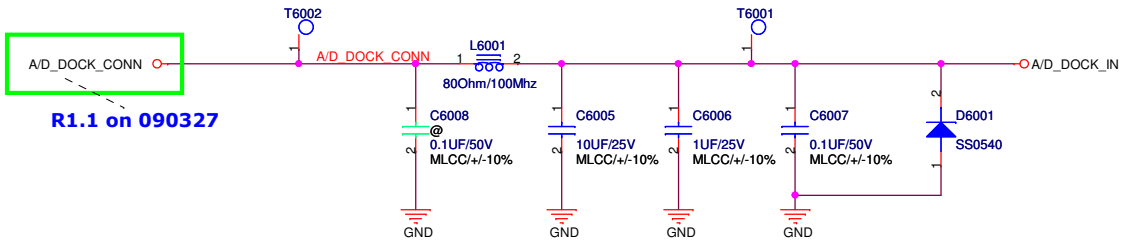
<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 58 of 93	

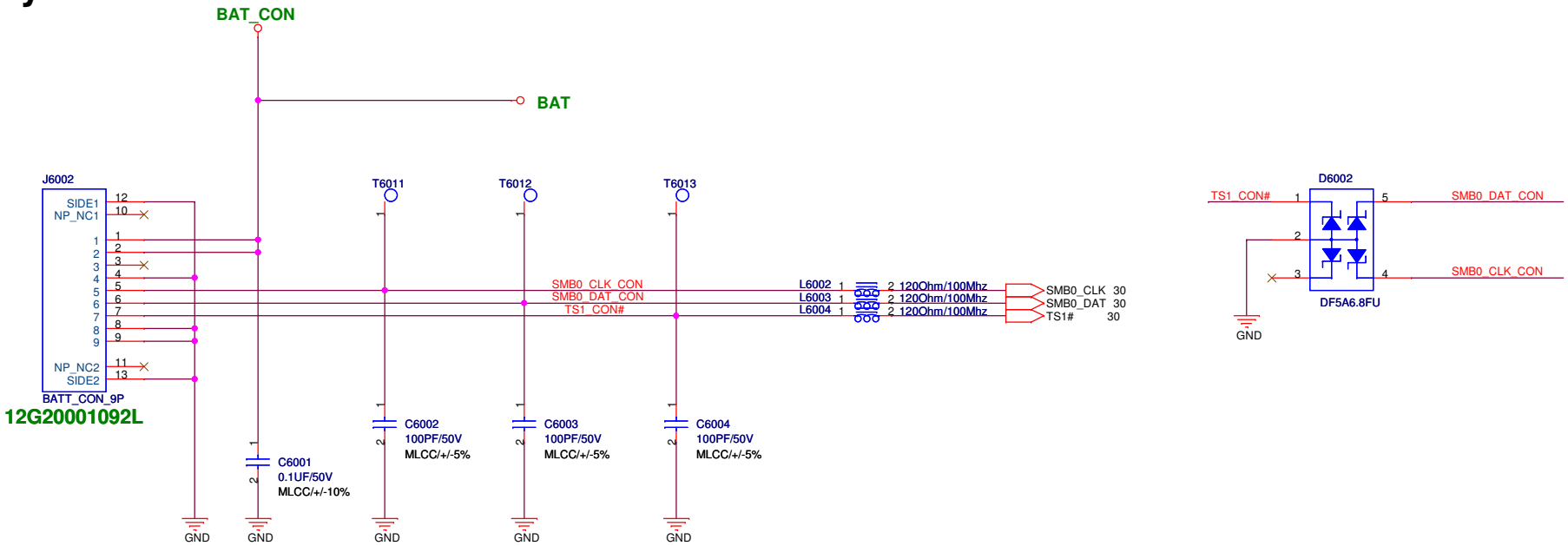
<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 59 of 93	

DC-IN



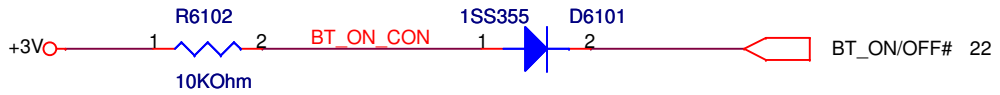
Battery Conn

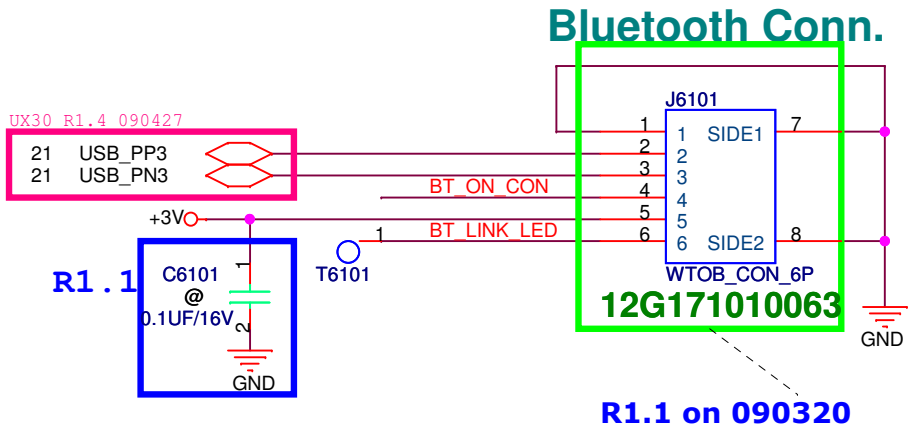


<Variant Name>

ASUSTeK COMPUTER INC	Title : DC DC&BATT CONN	
	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 1.4
Date: Friday, May 08, 2009	Sheet 60 of 93	

BT CON





<Variant Name>

ASUSTeK COMPUTER INC	Title : BT BLUETOOTH CONN	
	Engineer: Uei Lee & Hacken	
Size A	Project Name UX30 MB	Rev 1.4
Date: Friday, May 08, 2009	Sheet 61 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 62 of 93	

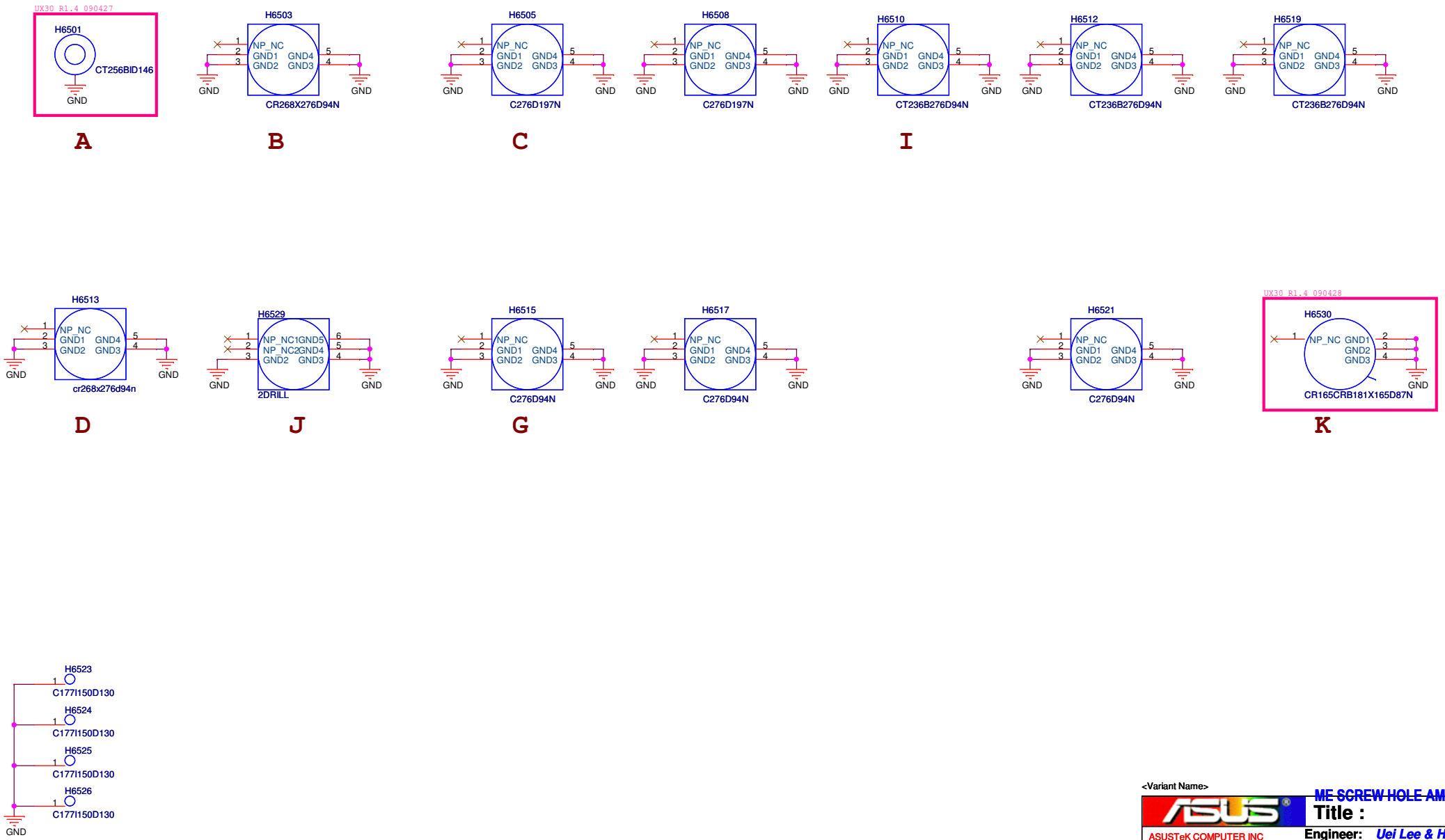
<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 63 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 64 of 93	

Screw Hole & SMT Nut



<Variant Name>

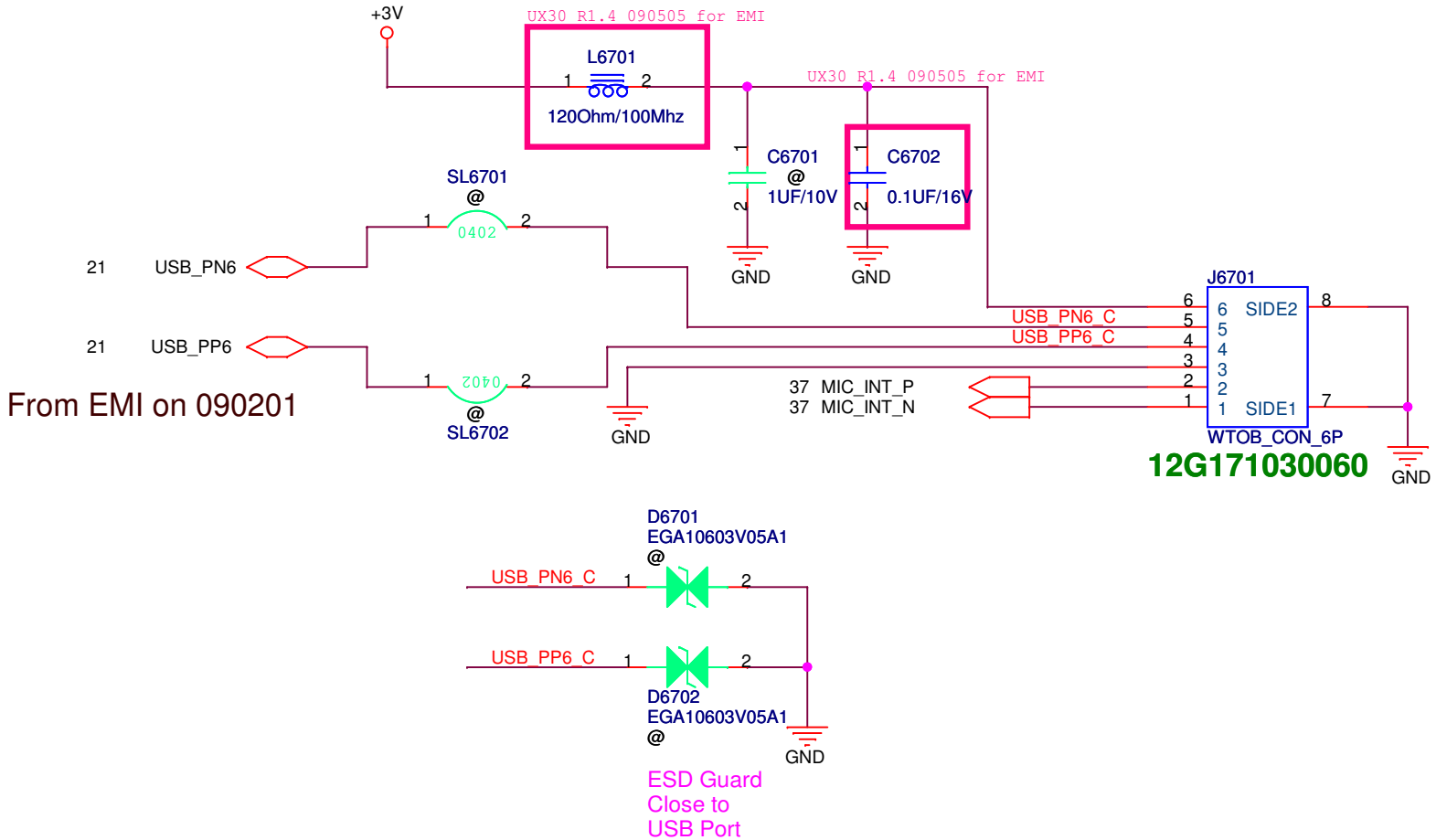
ASUSTeK COMPUTER INC	Title : ME SCREW HOLE AMT NUT	
	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 1.4
Date: Tuesday, April 28, 2009	Sheet 65 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 66 of 93	

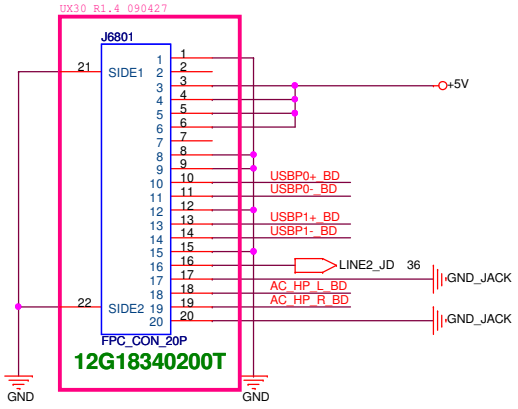
Camera Module

3V CAMERA MODULE



<Variant Name>

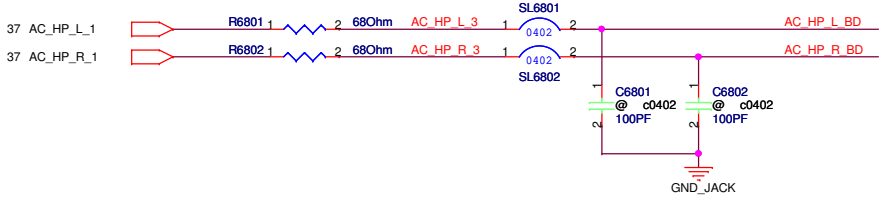
ASUSTeK COMPUTER INC	Title : CMOS CAMERA	
	Engineer: Uei Lee & Hacken	
Size A	Project Name UX30 MB	Rev 1.4
Date: Friday, May 08, 2009	Sheet 67 of 93	



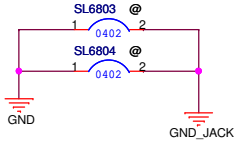
USB POWER

USB PORT X2

AUDIO

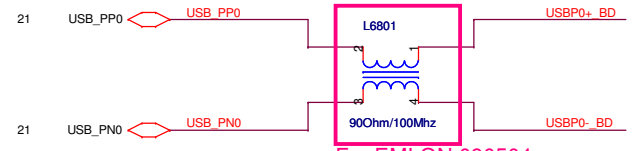


For EMI

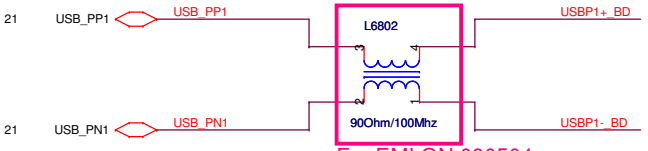


From EMI on 090202

USB PORT X2



For EMI ON 090504



For EMI ON 090504

<Variant Name>

ASUSTeK COMPUTER INC	Title : I/O BOARD CON	
	Engineer: Uei Lee & Hacken	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
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SYSTEM

+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,57,82
+VCC_GMCH	+VCC_GMCH	14
+VGFX_CORE	+VGFX_CORE	14
+3VS	+3VS	3,8,11,12,15,17,21,22,23,24,29,30,31,32,36,44,45,46,47,50,51,53,56,57,80,87,88
+VCORE	+VCORE	4,5,80
+1.5VS	+1.5VS	4,15,20,23,36,37,53,57,84
+5V	+5V	52,57,68,87
+5VS	+5VS	23,30,36,45,47,50,51,56,57,80,84,87
+3VA	+3VA	20,30,56,81,85
+VCC_RTC	+VCC_RTC	20,23
+3V	+3V	21,33,42,46,53,57,61,67,87
+3VSUS	+3VSUS	20,21,22,23,30,33,37,53,56,57,81,87,88
+5VSUS	+5VSUS	23,56,81,82,83,85,87
+3VPLL	+3VPLL	30
+3VACC	+3VACC	30
+3VA_EC	+3VA_EC	30,31,56
+5VS_AMP	+5VS_AMP	36
+12V	+12V	37,87
+12VS	+12VS	22,46,53,87
AC_BAT_SYS	AC_BAT_SYS	46,80,81,82,83,85
BAT	BAT	60,85
+5VA	+5VA	81
A/D_DOCK_IN	A/D_DOCK_IN	60,85
BAT_CON	BAT_CON	60,85

<Variant Name>

ASUSTeK COMPUTER INC

Title : POWER SOURCE

Engineer: Uei Lee & Hacken

Size	Project Name	Rev
A	UX30 MB	1.4

Date: Friday, May 08, 2009 Sheet 69 of 93

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 70 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 71 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 72 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 73 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 74 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 75 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 76 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 77 of 93	

<Variant Name>

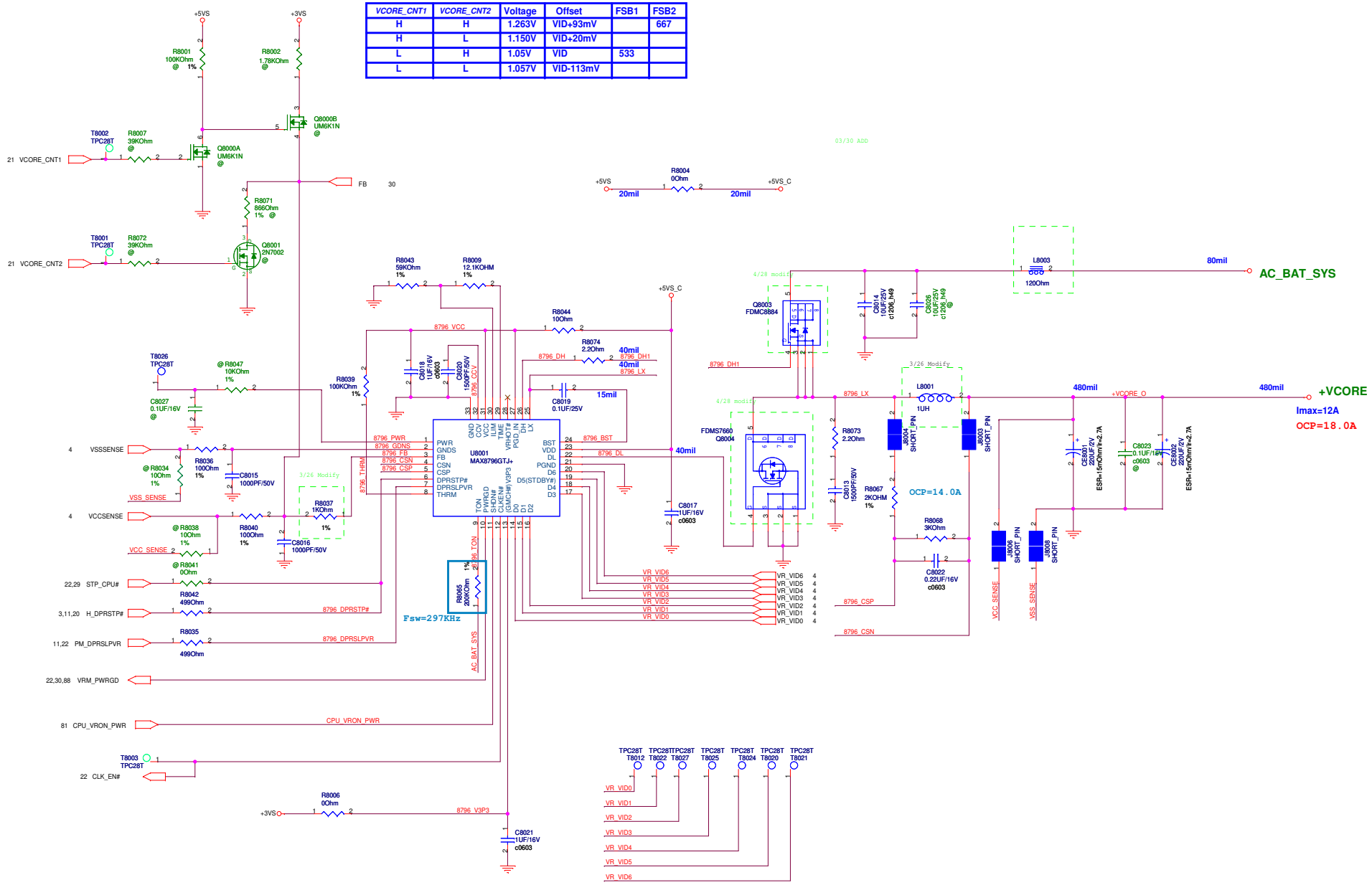
ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 78 of 93	

<Variant Name>

ASUSTeK COMPUTER INC	Title :*	
	Engineer: Uei Lee & Hacken	
Size: A	Project Name: UX30 MB	Rev: 1.4
Date: Monday, April 27, 2009	Sheet 79 of 93	

CPU
VID=1.05V

VCORE_CNT1	VCORE_CNT2	Voltage	Offset	FSB1	FSB2
H	H	1.263V	VID+93mV		667
H	L	1.150V	VID+20mV		
L	H	1.05V	VID	533	
L	L	1.057V	VID-113mV		



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE

Engineer: CH

Size	Project Name	Rev
C	UX30 MB	1.4

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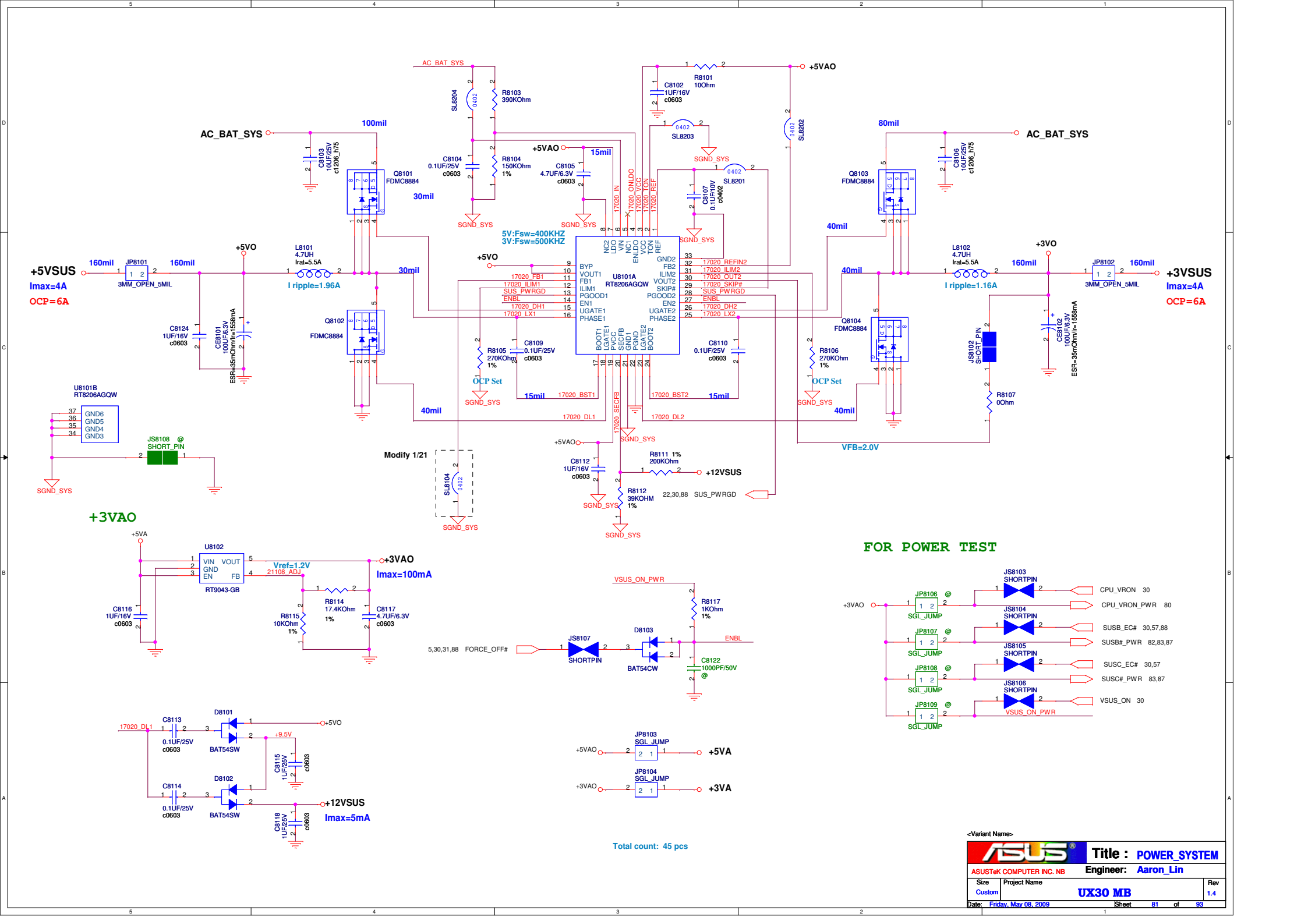
AC_BAT_SYS
+5VAO
+5VSUS
Imax=4A
OCP=6A
+3VSUS
Imax=4A
OCP=6A
+5VO
+3VO
U8101A
RT8206AGQW
U8101B
RT8206AGQW
5V:Fsw=400KHZ
3V:Fsw=500KHZ
I ripple=1.96A
I ripple=1.16A
OCP Set
VFB=2.0V
+12VSUS
22,30,88 SUS_PWRGD
Modify 1/21
+3VAO
U8102
RT9043-GB
Vref=1.2V
+3VAO
Imax=100mA
5,30,31,88 FORCE_OFF#
VSUS_ON_PWR
ENBL
+12VSUS
Imax=5mA
+5VA
+3VA
Total count: 45 pcs
FOR POWER TEST
CPU_VRON 30
CPU_VRON_PWR 80
SUSB_EC# 30,57,88
SUSB#_PWR 82,83,87
SUSC_EC# 30,57
SUSC#_PWR 83,87
VSUS_ON 30
<Variant Name>
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer: Aaron_Lin
Size Custom
Project Name UX30 MB
Rev 1.4
Date: Friday, May 08, 2009
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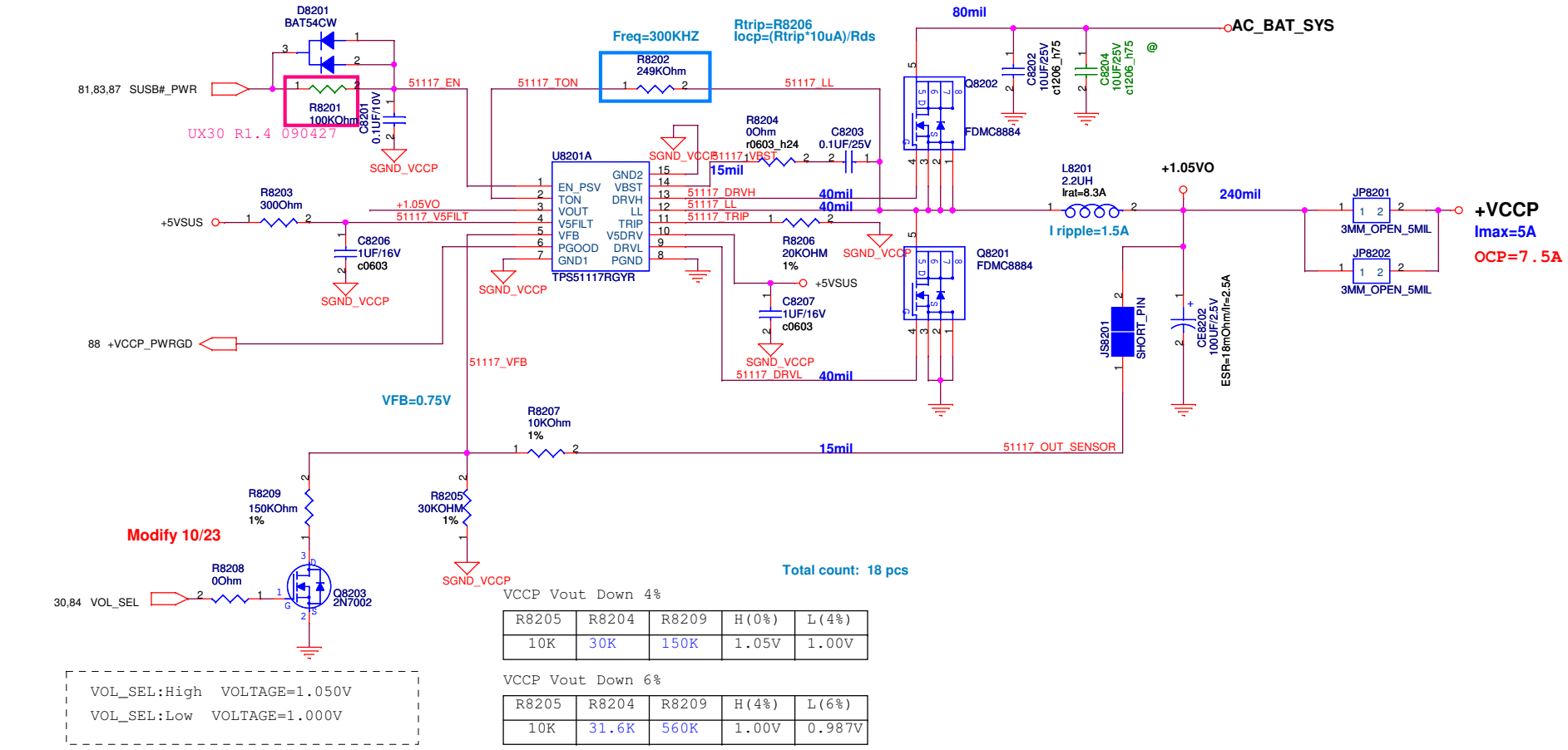
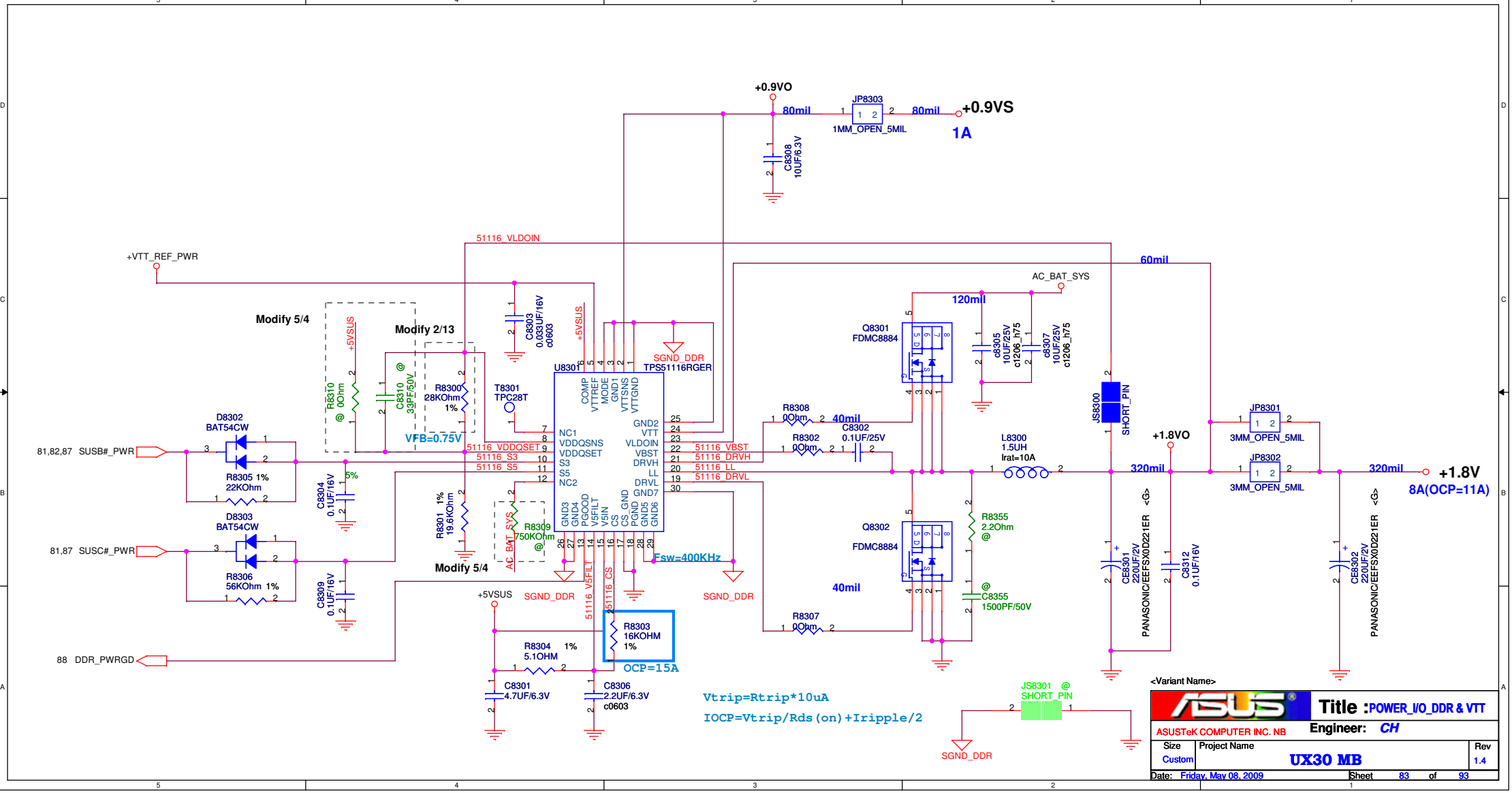


<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_+VCCP	
	Engineer: Aaron_Lin	
Size B	Project Name UX30 MB	Rev 1.4
Date: Friday, May 08, 2009	Sheet 82 of 93	



ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_DDR & VTT

Engineer: CH

Size	Project Name	Rev
Custom	UX30 MB	1.4

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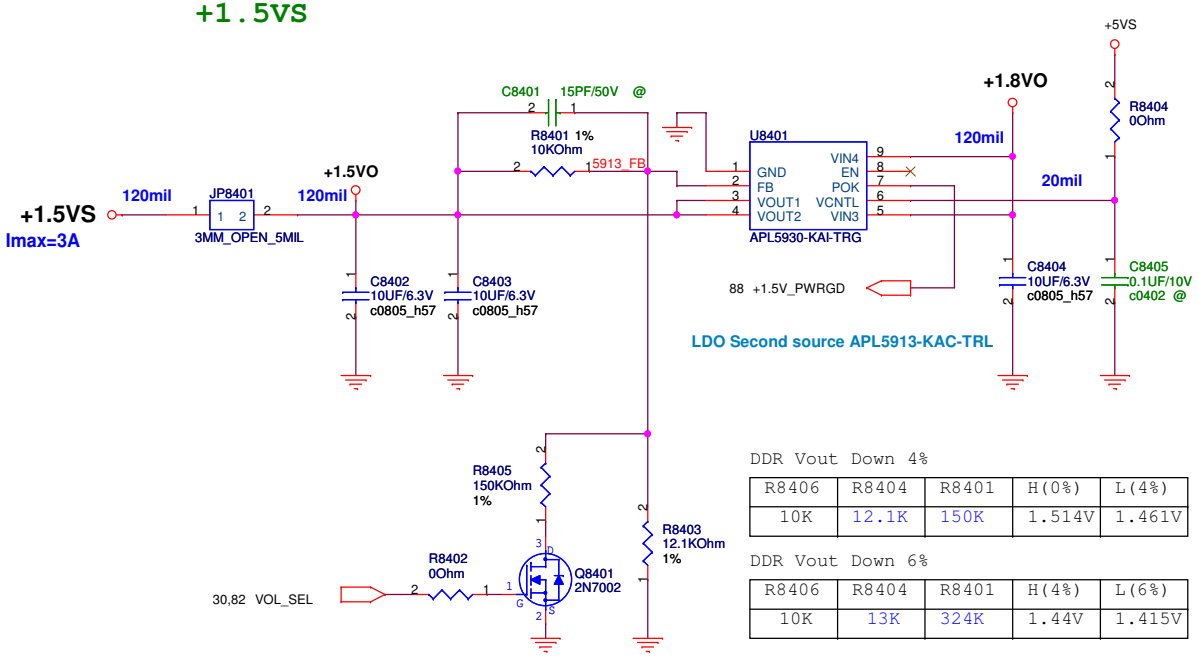
Total count: 29 pcs

+1.5VS



VOL_SEL:High VOLTAGE=1.51V

VOL_SEL:Low VOLTAGE=1.46V

DDR Vout Down 4%

R8406	R8404	R8401	H(0%)	L(4%)
10K	12.1K	150K	1.514V	1.461V

DDR Vout Down 6%

R8406	R8404	R8401	H(4%)	L(6%)
10K	13K	324K	1.44V	1.415V

Total count: 7 pcs

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_+1.5VS	
	Engineer: Aaron_Lin	
Size: B	Project Name: UX30 MB	Rev: 1.4
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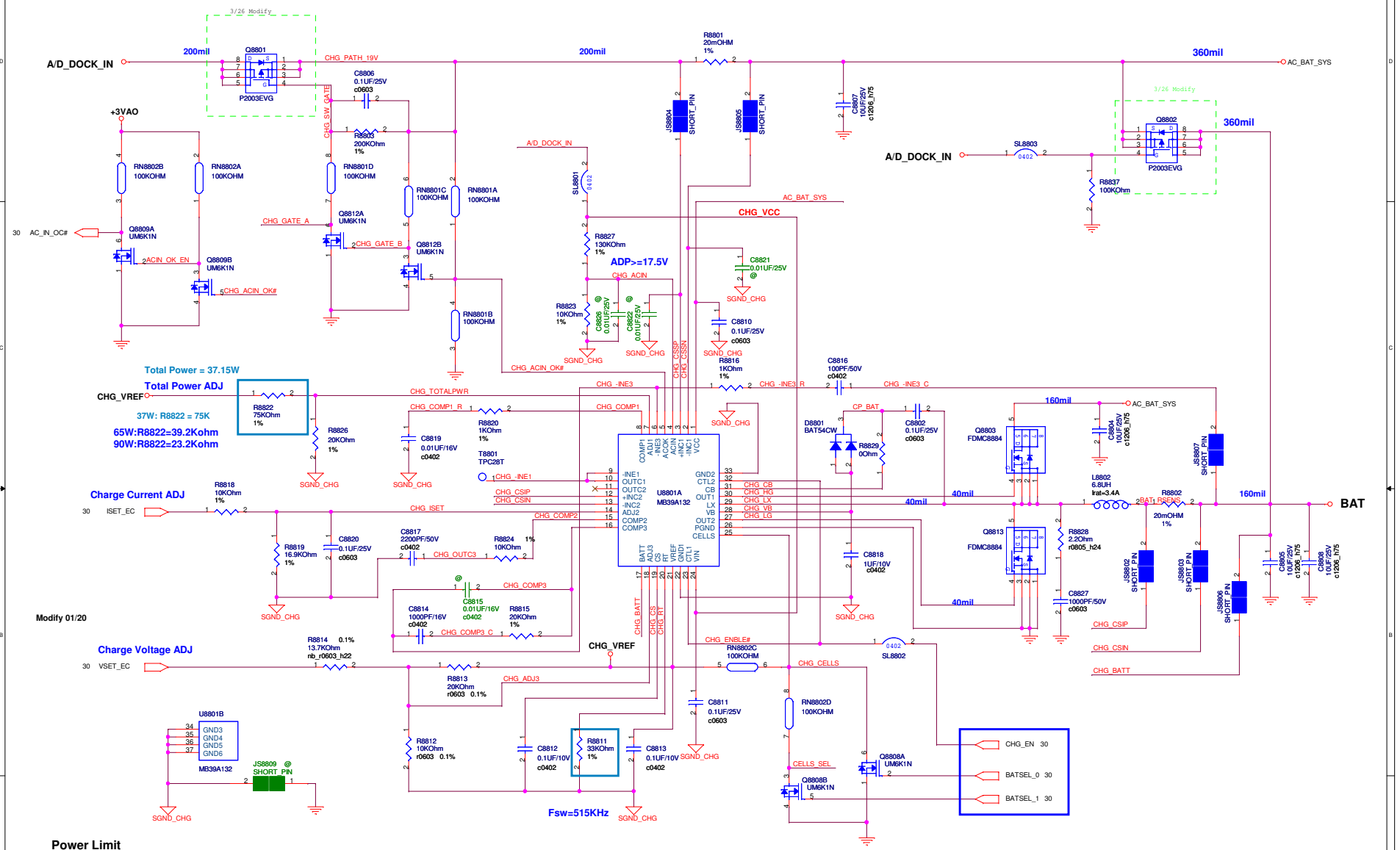

Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202

ASUSTeK COMPUTER INC. NB3

Title : CHARGER_202

Engineer:

Size	Project Name	Rev
Custom	UX30 MB	1.4

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BATTERY IN DETECT

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_DETECT	
	Engineer: Aaron_Lin	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
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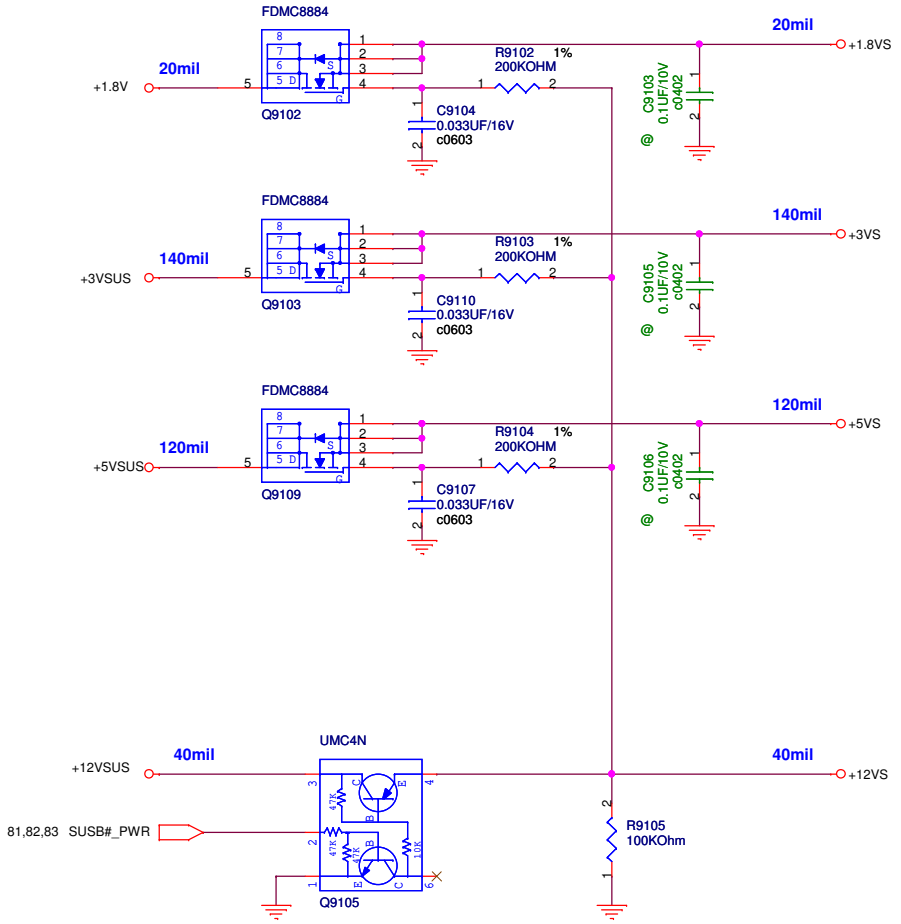
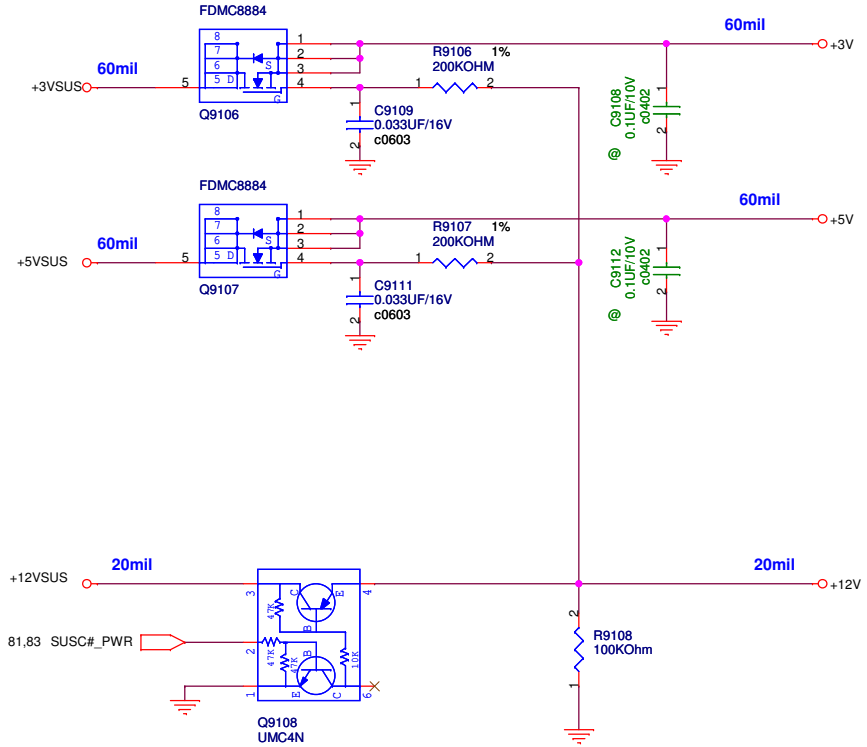
SUSB#_PWR POWER



Total count: 19 pcs

SUSC#_PWR POWER



<Variant Name>

ASUS	Title : POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB	Engineer: Fred Shih	
Size B	Project Name UX30 MB	Rev 1.4
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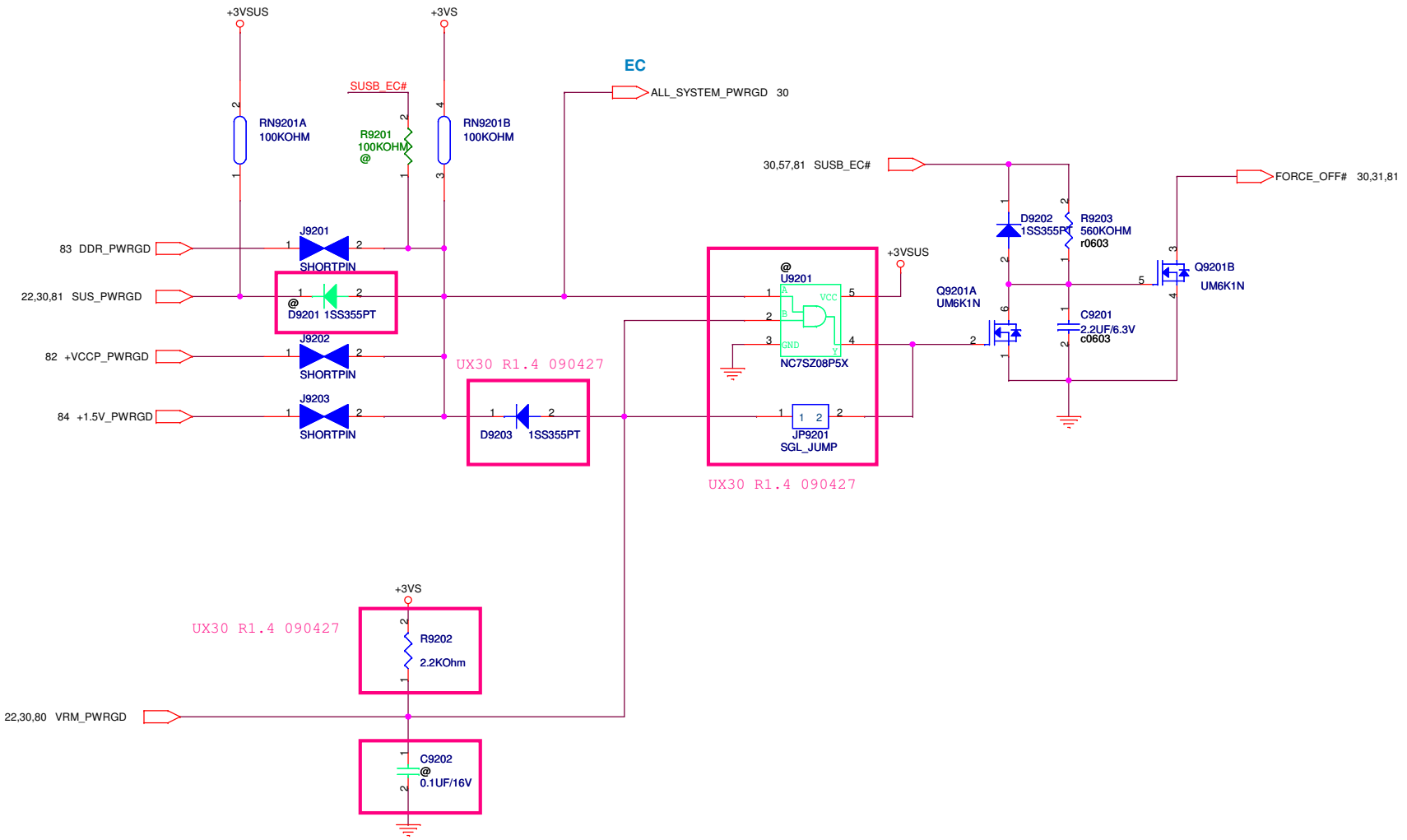
POWER GOOD DETECTER



Total count: 8 pcs

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Aaron_Lin	
Size: B	Project Name: UX30 MB	Rev: 1.4
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AC_BAT_SYS	AC_BAT_SYS	46,80,81,82,83,85
BAT	BAT	60,85
BAT_CON	BAT_CON	60,85
+3VAO	+3VAO	81,85
+5VA	+5VA	81
+3VA	+3VA	20,30,56,81,85
+5VAO	+5VAO	81
+5VO	+5VO	81
+5VSUS	+5VSUS	23,56,81,82,83,85,87
+5V	+5V	52,57,68,87
+5VS	+5VS	23,30,36,45,47,50,51,56,57,80,84,87
+3VO	+3VO	81
+3VSUS	+3VSUS	20,21,22,23,30,33,37,53,56,57,81,87,88
+3V	+3V	21,33,42,46,53,57,61,67,87
+3VS	+3VS	3,8,11,12,15,17,21,22,23,24,29,30,31,32,36,44,45,46,47,50,51,53,56,57,80,87,88
+12VSUS	+12VSUS	81,87
+12V	+12V	37,87
+12VS	+12VS	22,46,53,87
+1.8VO	+1.8VO	83,84
+1.8V	+1.8V	8,9,11,14,19,57,83,87
+1.8VS	+1.8VS	15,87
+0.9VS	+0.9VS	9,57,83
+0.9VO	+0.9VO	83
+1.05VO	+1.05VO	82
+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,57,82
+1.5VO	+1.5VO	84
+1.5VS	+1.5VS	4,15,20,23,36,37,53,57,84
+VCORE	+VCORE	4,5,80
A/D_DOCK_IN	A/D_DOCK_IN	60,85

Total sum count: 236 pcs

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_SIGNAL

Engineer: Aaron_Lin

Size	Project Name	Rev
Custom	UX30 MB	1.4

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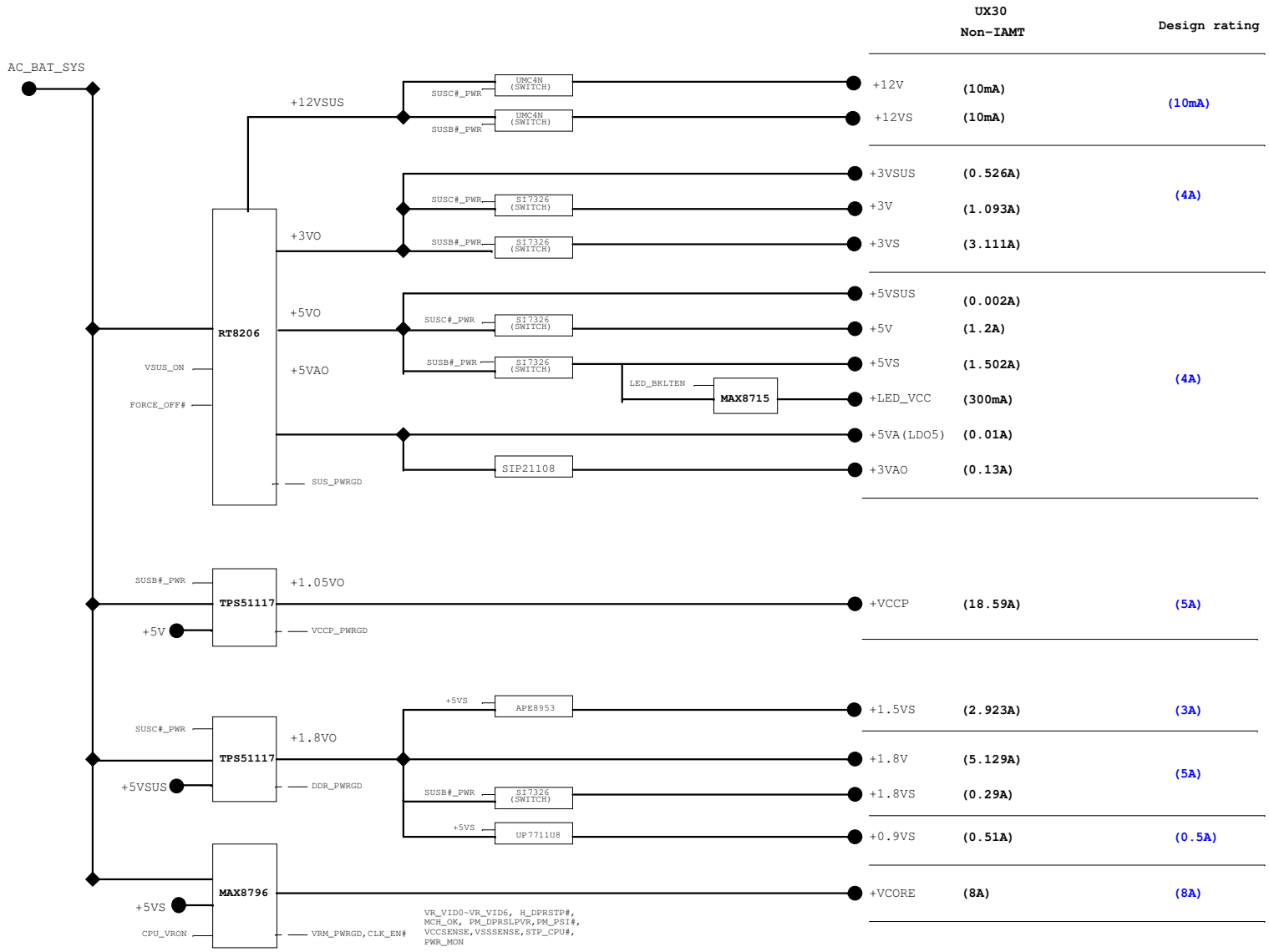

<Variant Name>

ASUS	Title : POWER_FLOWCHART	
ASUSTeK COMPUTER INC. NB	Engineer: Aaron_Lin	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
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Modify 2/13

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_LED_VCC BOOST	
	Engineer: Aaron_Lin	
Size: Custom	Project Name: UX30 MB	Rev: 1.4
Date: Friday, May 08, 2009	Sheet 91 of 93	

E30 MB R1.1 Change List

1. Open Mask of JP3002 , JP3003 , JP8103 , JP8104 for SMT
2. Put on R2902 , C2913 , C2914 , JP3001 for SMT
3. Change R2911 from 22 Ohm to 10 Ohm for EA measure fail
4. Change R2910 from 22 Ohm to 10 Ohm and change net to CLK_SEL_48# for EA measure fail
5. Change Q4602 from SI3456BDV to SI3460BDV and add R4601 with 200K to GND for clear stocks
6. Change Q5302 from SI3456BDV to SI3460BDV and add R5307 with 200K to GND for clear stocks
7. Swap SL3621 and SL3622 for ACZ_Audio level change
8. Swap J4201 Pin 10 / 11 NET Name (SDCDN/XDWRN / SDWP/XDCLE/MSCLK) for SD Detection
9. Remove U3102 and C3105 for LID_SW# function for error design on MB
10. Add Q3704 and R3704 for Audio Level shift from +1.5VS to +3VS
11. Change BT Connector J6101 from 10 Pin to 6 Pin for N10 common use
12. Swap RTC Battery Connector CON2001 Pin Define for RTC common pin define
13. Change X3301 from 07G010S22500 to 07G010212502
14. Change R2904 , R2906 , R2907 from 22 Ohm to 10 Ohm for EA measure
15. Change J5601 from 6 pin to 8 pin and change pin define for PM spec change
16. Remove J4701 and related net for SR2 change
17. Change J3401 from 12G14830108D to 12G148611083 for ID design
18. Change J3701 , J3702 from 12G171030022 to 12G17100002C for Cost down
19. Change CON4601 from 12G170040308 to 12G170040308 for Cost down
20. Add H6530 for ME screw hole
21. Change J5604 from 12G171030140 to 12G171030121 for ID design
22. Remove J5603 , J6001 and change to J5602 on DC-IN BD for ME cost down
23. Change D3401 , D3402 , D5201 from 07G001250010 to 07G028075010 for EE Cost down
24. Change SL4602 to L4605 for EMI test
25. Add L8003 for EMI test
26. Delete Num_LED# function for Spec change

ASUS	Title : HISTORY	
<OrgName>	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 1.4
Date: Monday, April 27, 2009	Sheet 92 of 93	

UX30 MB R1.4 Change List

1. Swap USB D+ , D- of BT on Page 61
2. Add C4710 , R4704 and C4711 , R4705 on Hsync and Vsync to improve CRT display quality on Page 47
3. Modify J5602 Pin 1 , 3 , 5 , 7 to GND for Apater use on Page 56
4. Change J6801 from 12G183402207 to 12G18340200T for cost down on Page 68
5. Change J5604 Pin 10 from +3VSUS to +3VA for Hall sensor on Page 56
6. Change H6501 from Screw Hole to a NUT for ME assembly on Page 65
7. Change PCB ID from R1.1 to R1.4 on Page 22
8. Add R2229 , R2231 on GPIO6 for On Board Memory Size and R2231 , R2232 on GPIO7 for Memory Vendor on Page 22
9. Change J5301 from 12G03010052K to 12G03010052P on Page 53
10. Change J0801 from 12G02502200F to 12G02502200S on Page 8
11. Change U3601 from 02G611005001 to 02G611005006 on Page 36

ASUS	Title : HISTORY_ER	
<OrgName>	Engineer: Uei Lee & Hacken	
Size B	Project Name UX30 MB	Rev 1.4
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